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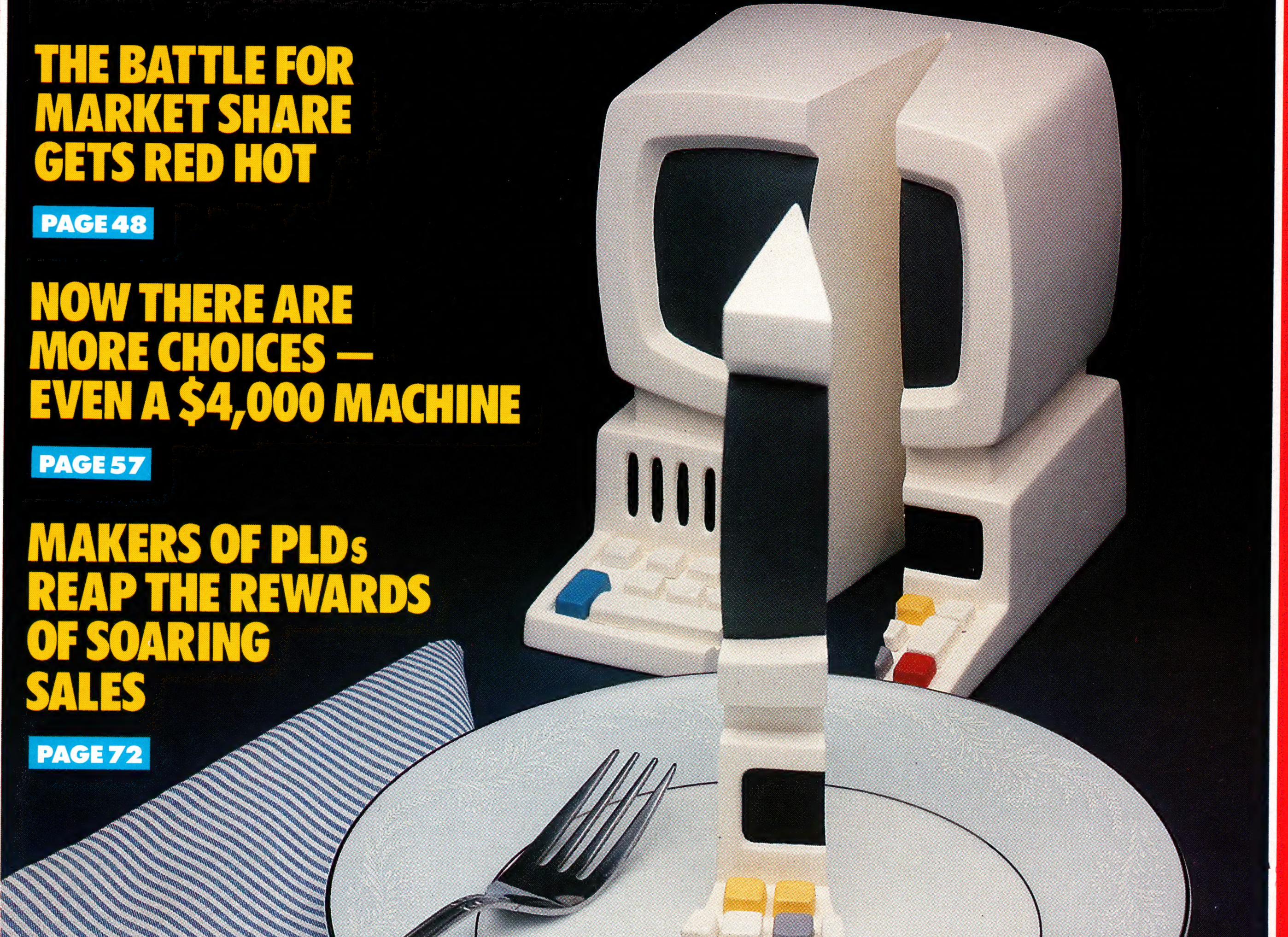

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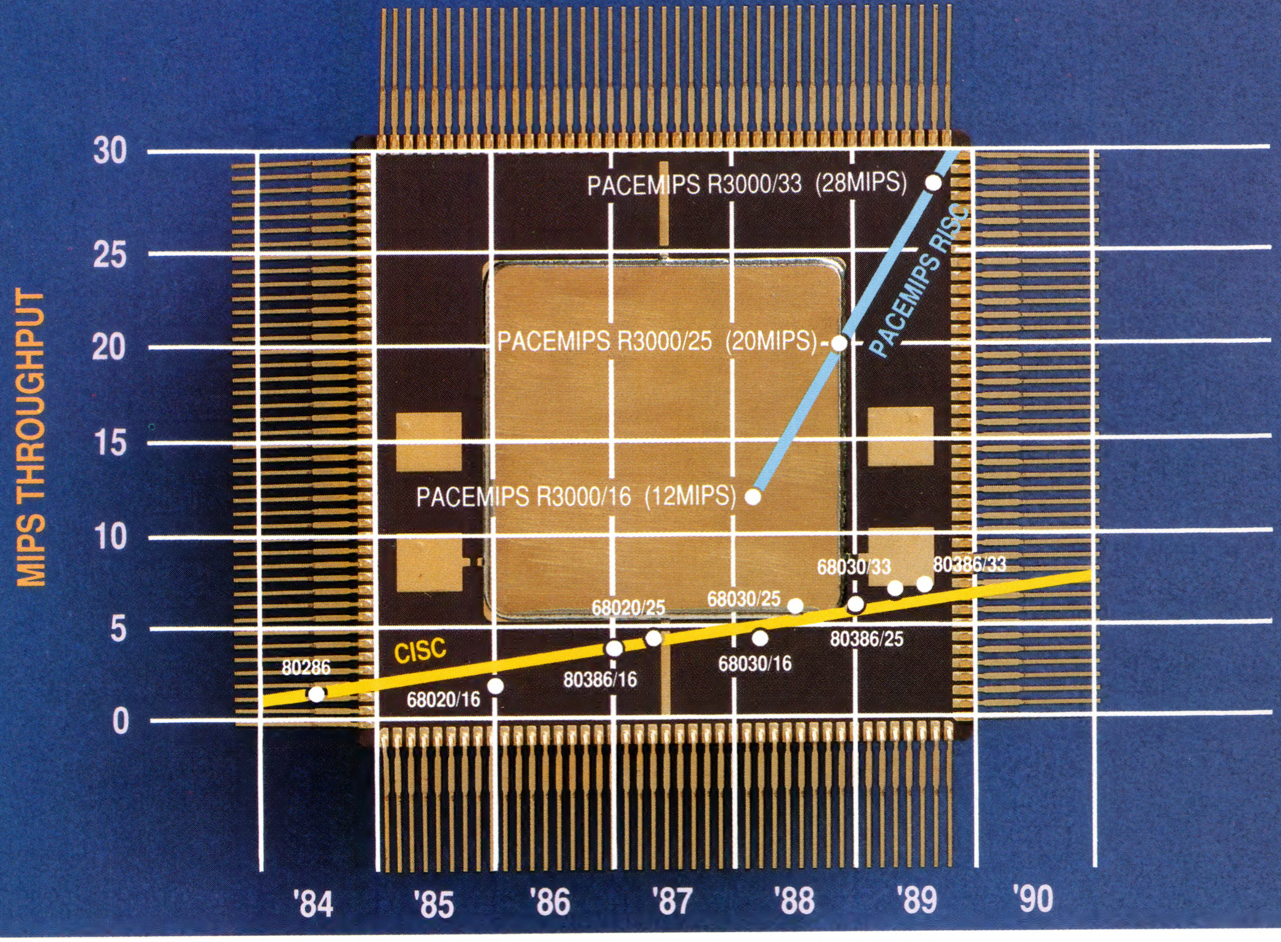

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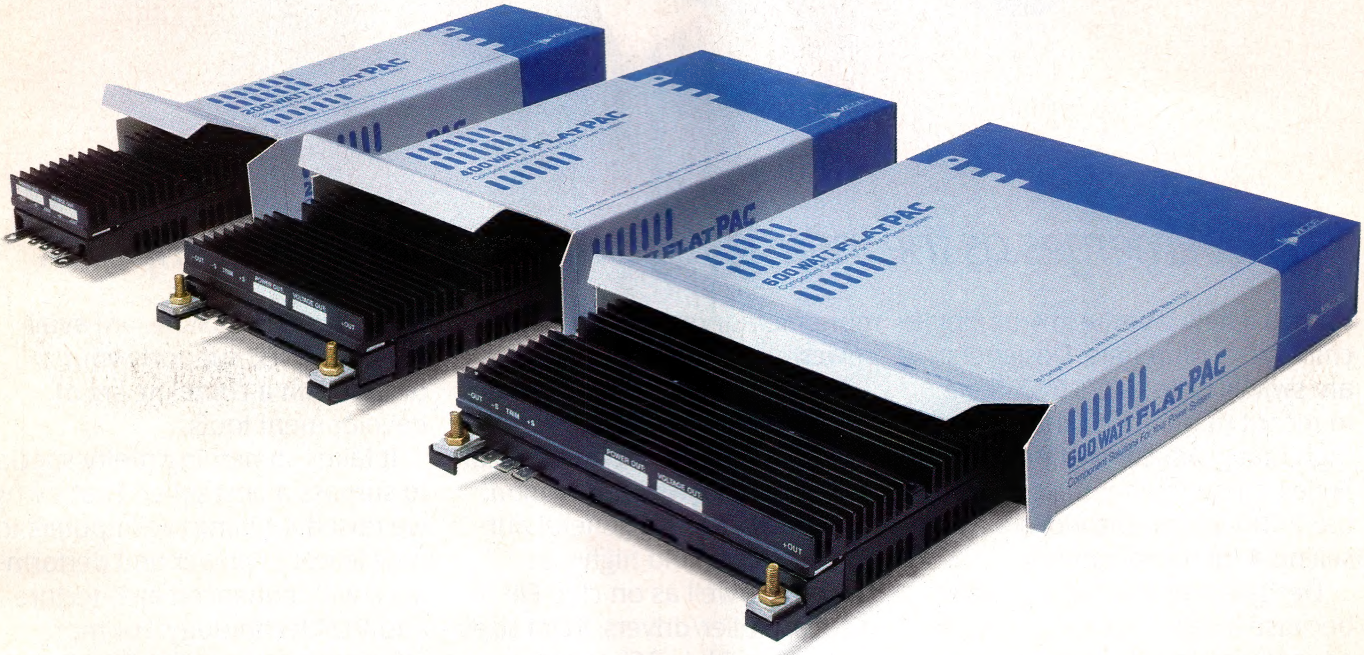

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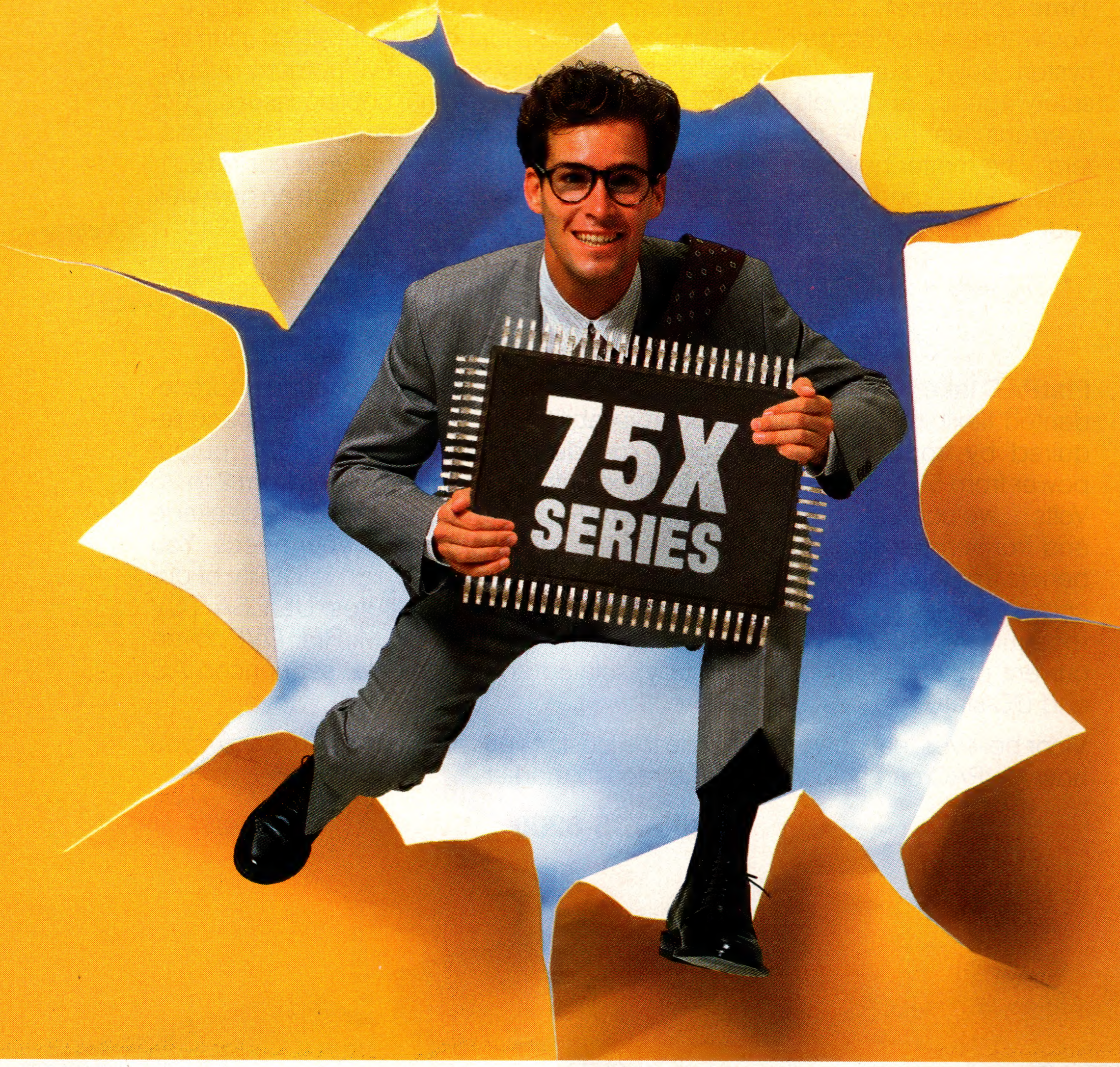

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OUTSIDE TRACK

Changing Times Dept.: The work station business will never be the same again, so if you are selling or buying, you'd better pay attention!

The work station business today is undergoing some big changes. So much so that some marketers compare it to the bold, exciting, "boffo" period when personal computers got a toehold on corporate computing. In keeping with the spirit of the times, it seems fitting that we borrow the boldly distinctive style of *PC Magazine* pundit John C. Dvorak to introduce our work station coverage (see p. 48):

From the One if By Mail, Two if By Lotto Machine Dept.: Convulsions in work station distribution methods are almost as big a story as the technology inside these machines. Competition on the **low end** from personal computers will probably force work station makers to sell their iron in ways that are S.O.P. for PCs, but which are **weird** for high-horsepower stuff. You can bet on some **innovative solutions** here. One thing for sure: it could be a completely **new ball game** with different players **even on the low end.**

Another part of the equation: Low price will be much less important than making sure that computing equipment and the networks it connects to are **bulletproof.** One reason is that work stations are increasingly wired into **big networks.** These systems serve as **all-important lifelines** for companies. Would **you** be willing to **low-ball** something that your whole business depended on? **Nobody** will want to shoulder the blame for a bargain-basement node crashing, especially if there is even a remote chance that the **whole network** could be **dragged down** with it. **From the The More Things Change the More They Stay the Same Dept.:** Several companies that make work stations show **good survival instincts.** They have figured out that they are really **not** in the work station business so much as in the **computer business.**

From the **Dodging the Elephants Dept.:** Given this, is there room for niche players in work stations? **Why not?** In nearly every product and service area, there are niche companies that somehow find ways to **keep from getting creamed** by the big guys. Why should work stations be different? **Look for successful niche players** to follow a simple strategy: stay close to your customers, but closer to your competitors.

Parting Advice Dept.: For work station vendors, **make friends** with MIS directors! They'll get control of the purse strings.

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LELAND TESCHLER

October 1989 Volume 62, Number 10

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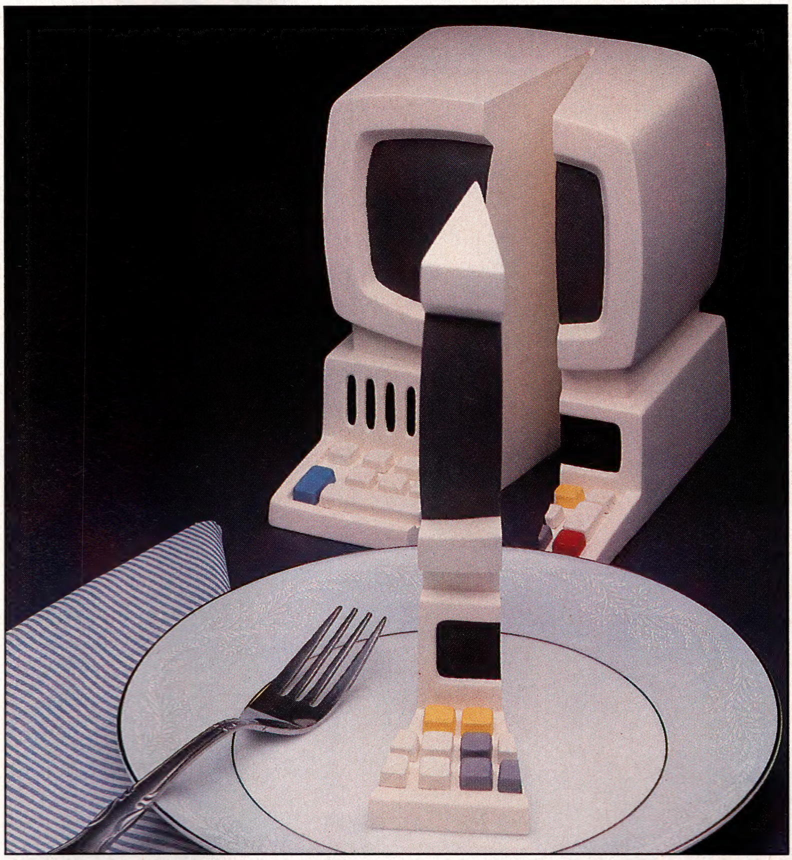

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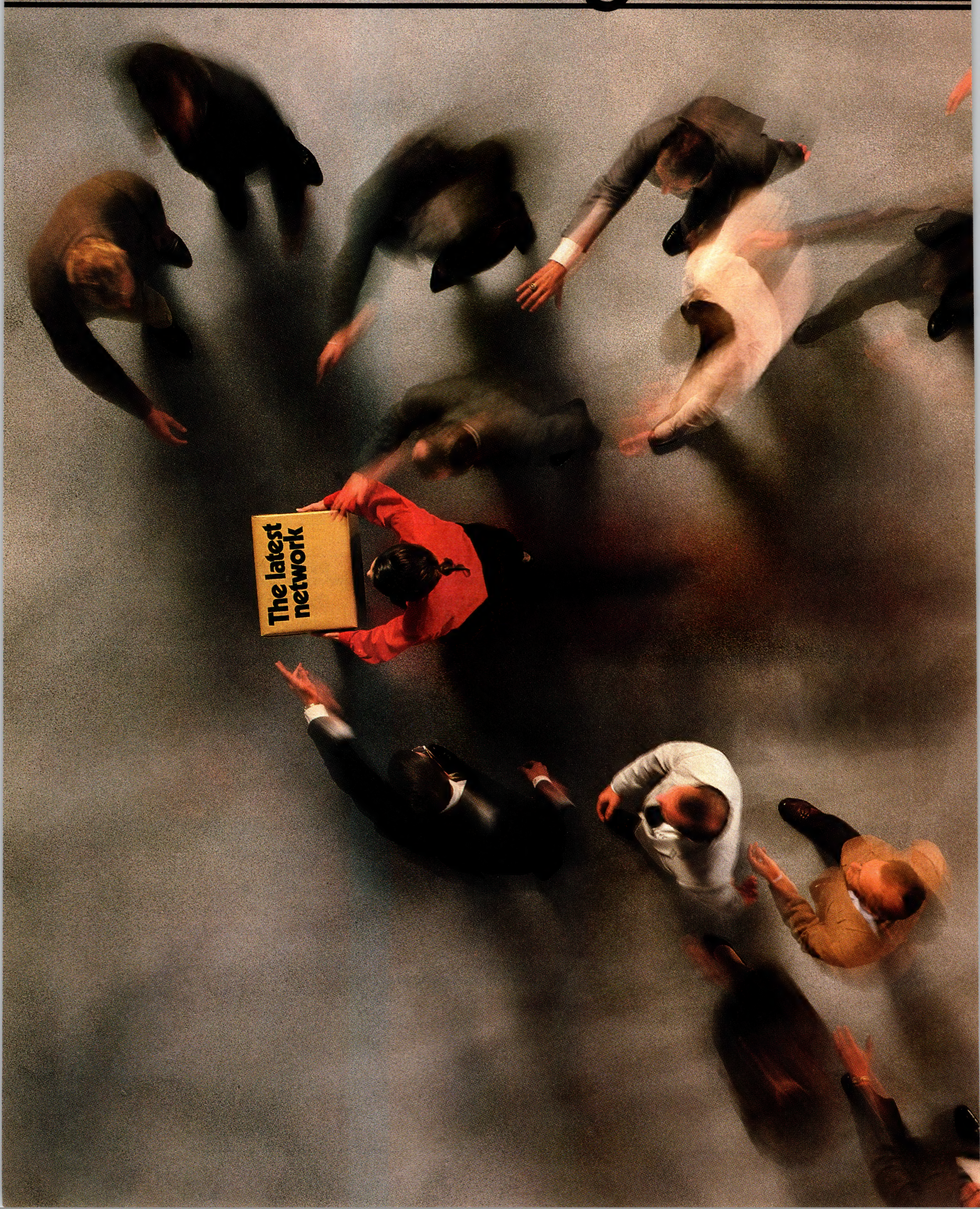

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LOW PAY MEANS A SHORTAGE OF ENGINEERS

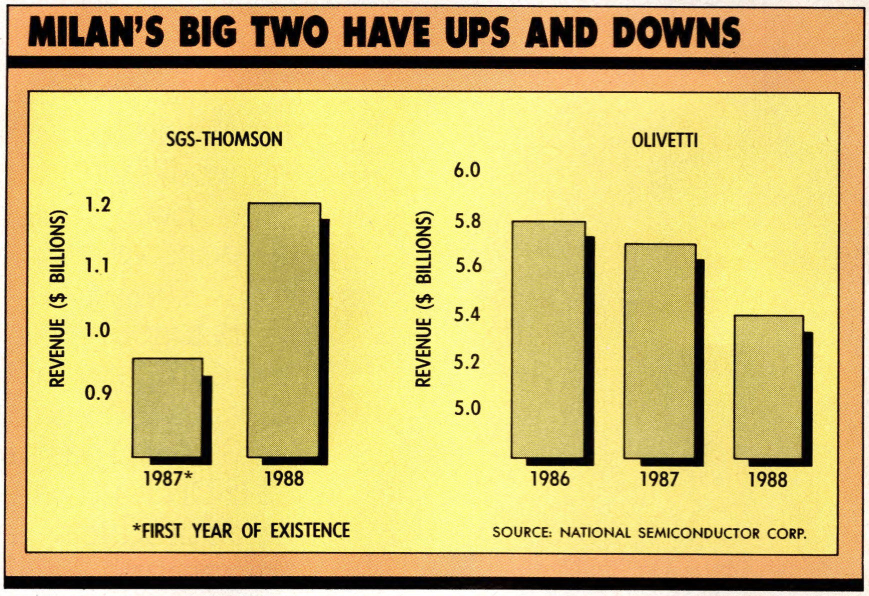
MILAN

The clothes are getting frillier, the restaurants are getting pricier, and the smog from perpetually stalled traffic is getting thicker in Milan, the capital of the Italian electronics industry. The medieval Italian city center, with its narrow winding streets, wasn't designed to handle automobile traffic, and it takes a hardy soul to brave the rush hour.

But for the people who toil in the electronics industry in Italy, those are mere distractions. They have other things to worry about—low pay, for example.

An electrical engineer who works in Italy is subject to a contract worked out for the entire Federation of Metalworkers union. The rules are ironclad: you start at about $15,000 a year net and, if you're good, you can work your way up to $40,000, according to figures supplied by union sources. Those on the fast track can become company directors, outdistancing the union guidelines to really make money. But only one in 100 manages to get that far.

With these disincentives, it's not surprising that the engineer shortage has hit Italy harder than elsewhere. Both of the big Milan-area electronics concerns—SGS-Thomson Microelectronics and Ing. C. Olivetti & Co. SpA—have begun training physicists and scientists who are working in engineering-related disciplines to do an engineer's job. "If we could," says an Olivetti senior executive, "we would hire every engineer who graduated from the university. It wouldn't matter what kind of training he had."


MILAN'S BIG TWO HAVE UPS AND DOWNS

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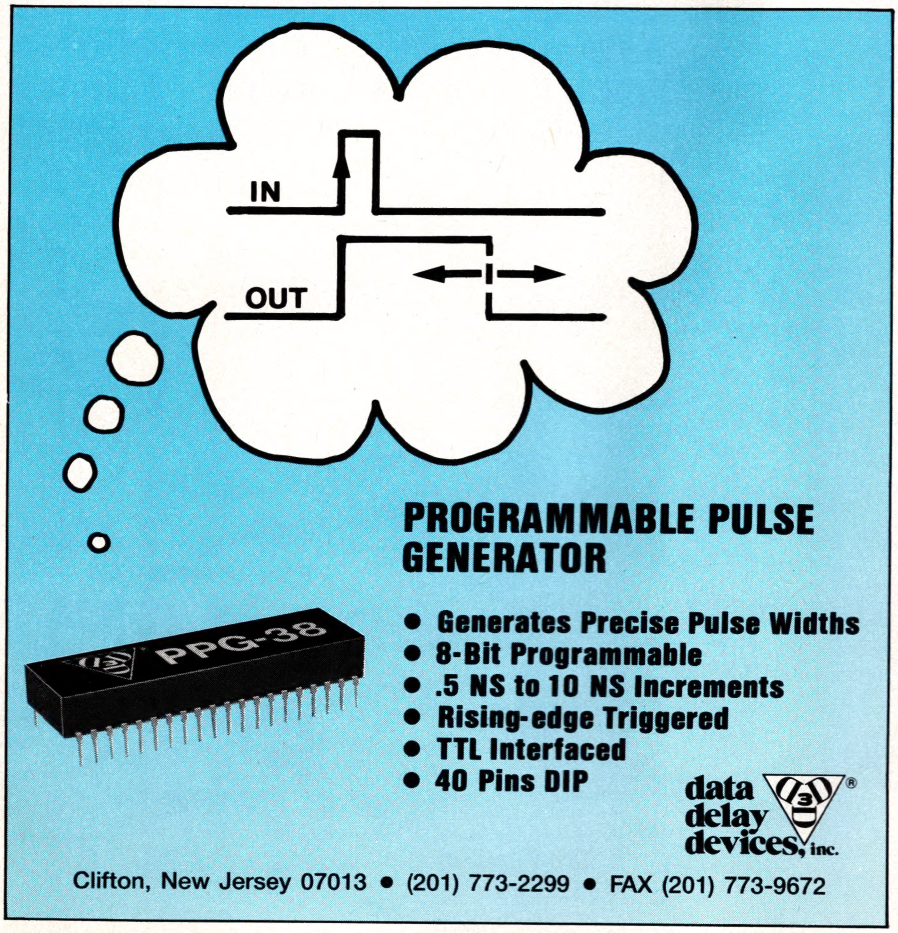
As if the shortage of technically qualified personnel weren't enough, there is also a shortage of help from the government. Although electronics companies elsewhere in Europe enjoy considerable government support, the industry in Italy can expect little from Rome. "The electronics industry here must create many things that are taken for granted elsewhere," says Olivetti vice president Ettore Morezzi.

So it's easy to see why those in the Italian electronics industry are said to be inspired by a singular devotion. Nowhere is that quality more evident than at Olivetti and SGS-Thomson, Italy's two largest electronics manufacturers. For Olivetti, that devotion is being put to the test by poor financial results, while SGS-Thomson faces the specter of a giant competitor setting up shop nearby.

Many Olivetti employees—including managing director Vittorio Cassoni—brave the clogged traffic to make the 50-mile northwest trek from Milan to the tree-lined paradise of the Olivetti campus at Ivrea. But the atmosphere at Ivrea has been gloomy recently. Late last summer, Olivetti chairman Carlo de Benedetti announced that the group's pretax profit had fallen 40% in the first half of this year, down to $732.2 million from last year's $1.22 billion.

Speaking at a shareholders' meeting intended to raise capital, de Benedetti talked about a "historic phase of discontinuity" that had affected the market for information technology in Italy. Most



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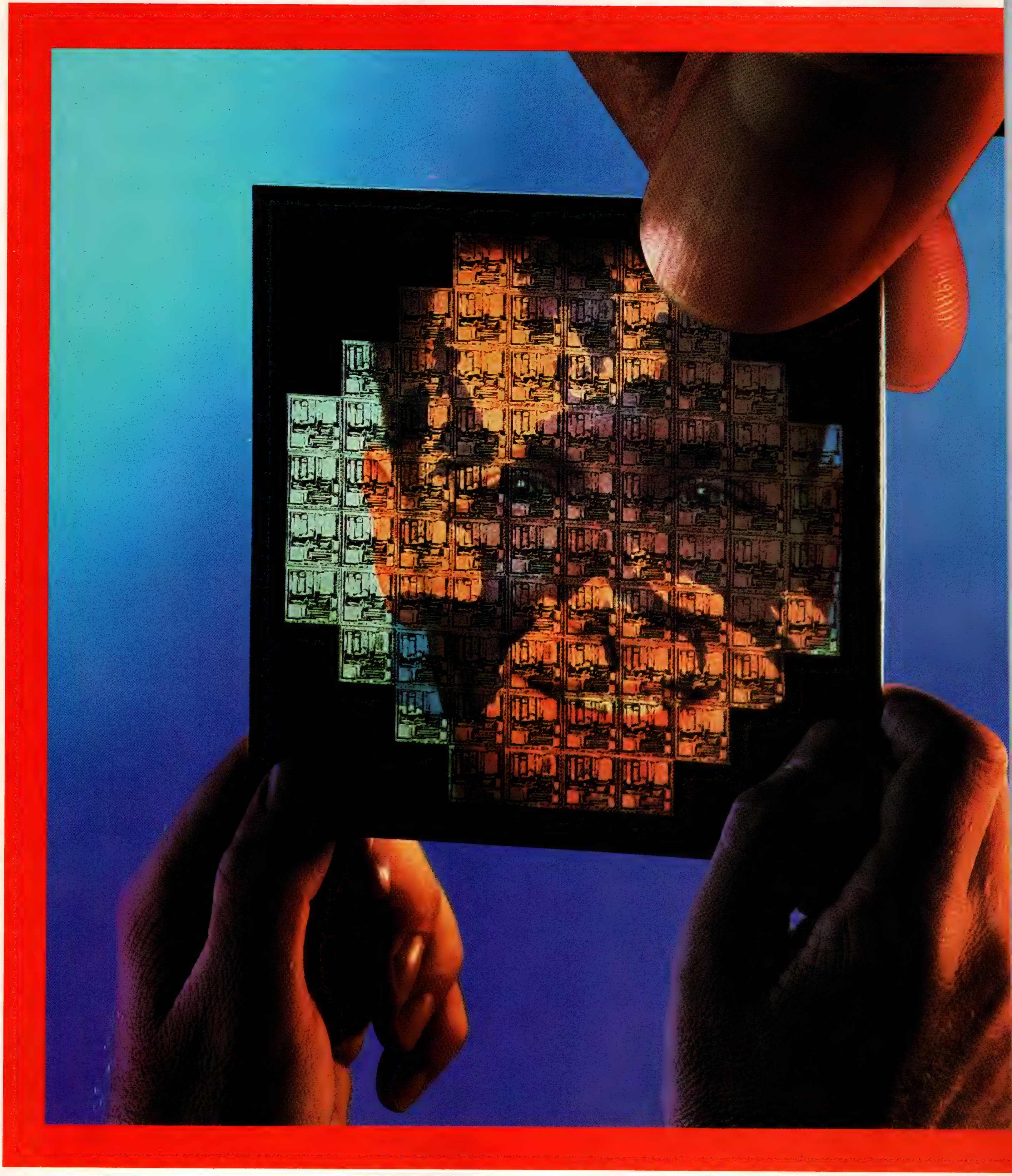

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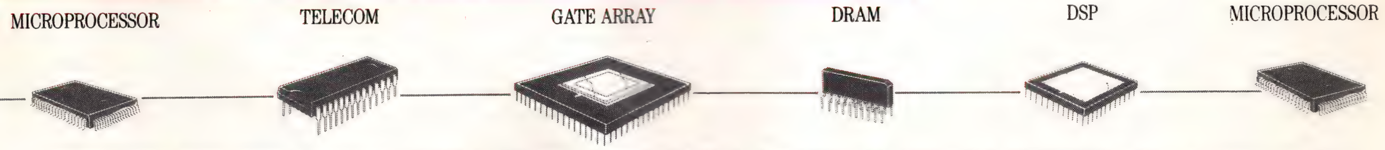

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people understood that he meant there was a slump, but that didn't prevent shareholders from unanimously voting an $856.3 million bond-and-stock issue. In fact, only two shareholders at the meeting even asked what the money was for.

"Ever since Carlo de Benedetti turned Olivetti around in 1979, he has enjoyed a singular degree of trust from his shareholders," explains Gianni Allavena, a Milan financial analyst. "It is true that this is the first time Olivetti has sought money from its investors since 1982. But after two successive bad years, how many company chairmen could expect such faith?"

At the meeting, managing director Cassoni announced that he intended to introduce by year's end a high-end personal computer based on Intel Corp.'s 80486 microprocessor, a secretarial work station, and a low-end personal computer.

FERVOR. Olivetti isn't the only electronics company in the Milan area to enjoy this kind of special fervor. Based at Agrate Brianza, about 15 miles northeast of the city center, SGS-Thomson has one of the lowest turnover rates in the world. "Many employees have worked for us since the beginning, back in 1957," one technician says with pride. And even though Texas Instruments Inc. is building a semiconductor plant in Italy's southeastern Abruzzi region, SGS-Thomson doesn't expect the new competition to lure away many trusted workers.

Employees boast of SGS-Thomson's solid position as Europe's No. 2 semiconductor supplier and its No. 12 ranking in worldwide sales. The company pulled in revenue of $1.2 billion in 1988. It sells more intelligent power devices than any other company. "But we're not part of a big group like [European rivals] Siemens or Philips," says vice president Enrico Villa. "We don't have a safety net."

Until recently, SGS-Thomson could count on help from the Italian government. Istituto di Ricostruzione Industriale, the Italian state agency that co-owns the company with France's state-owned Thomson-CSF, put $100 million into it last year after SGS-Thomson acquired the UK's Inmos Ltd. But the Italian government is faced with a ruinous budget deficit, and cuts are surely in store this year. Moreover, progressive-minded IRI president Romann Prodi is on the way out, and the new chief may not be as enthusiastic a supporter.

SGS-Thomson assures its growth by financing 60% of its research and development through internal investment. The company keeps profitability at a mere 10%, a strategy that led one German magazine to call it "the Japanese of Europe."

Research at the Agrate Brianza laboratory is good enough to attract some of the major work of the European Community Joint European Submicron Silicon Initiative's Joint Memory Project, which is intended to produce a European nonvolatile dynamic random-access memory. "In France, research tends to be separated from production," says Villa. "Our research is always linked to a specific line of production. This philosophy has put Agrate, at least for the present, at the avant-garde of current research."

SGS-Thomson employees are proud of their work. In fact, they claim that competitors have difficulty matching the touch of famous Italian creativity that goes into the company's products.

"Every year one of our major clients is approached by the Japanese," Villa recounts. "They offer that client a chip with an identical data sheet to the one that we sell, but with a lower price. SGS-Thomson can't match the Japanese offer, and the client switches. Yet every year, the Japanese chips fail because their design can't stand up to varying heat generation. The client realizes that there is something that isn't indicated on the data sheet, and he switches back to us." *–Andrew Rosenbaum*

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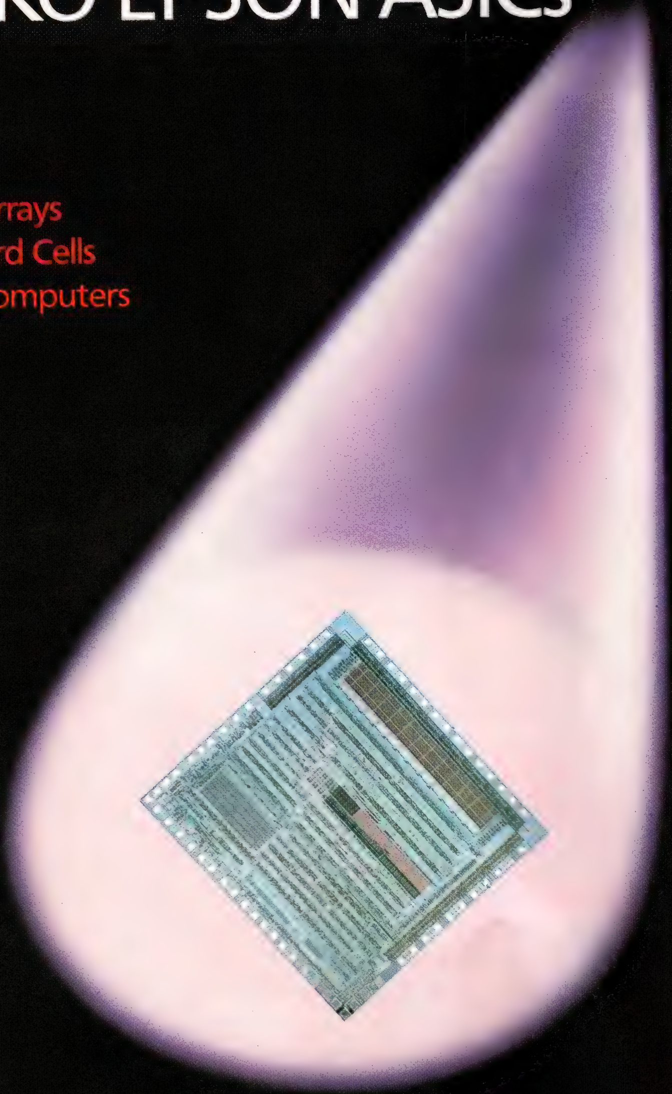

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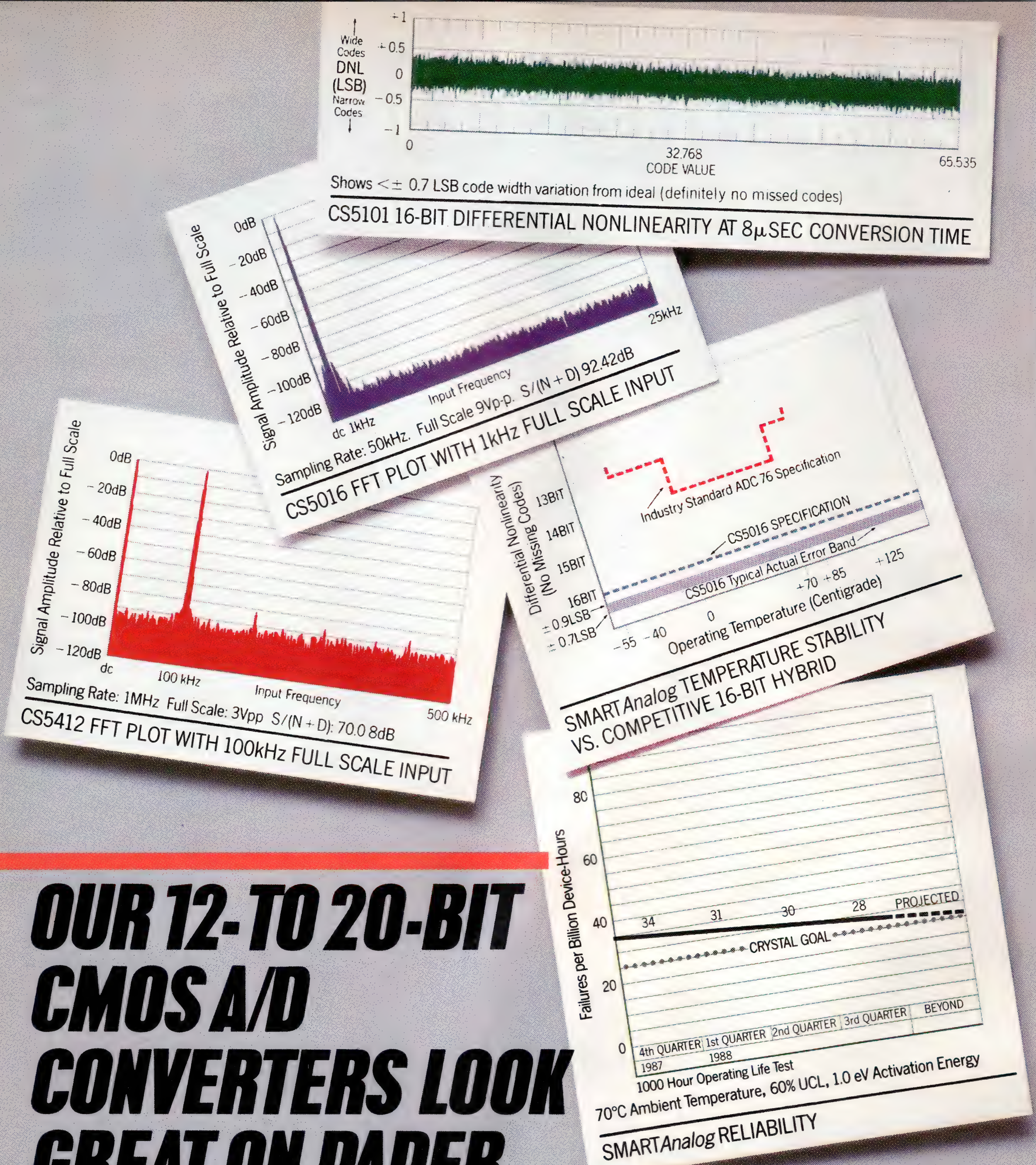

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DEVICE	CS5012	CS5014	CS5016	CS5101	CS5102	CS5317	CS5324	CS5326	CS5328	CS5412	CS5501	CS5503
Resolution (Bits)	12	14	16	16	16	16	>20	16	18	12	16	20
Conversion Time (µs)	7	14	16	8	80	-	-	-	-	1.25	-	-
Throughput Speed (kHz)	100	56	50	100	10	20	>1kHz	48	48	1MHz	4	4
Input Bandwidth (kHz)	-	-	-	-	-	10	500Hz	22	22	4MHz	10Hz	10Hz
Linearity Error (±% F.S.)	.006	.002	.001	.0015	.0015	-	-	-	-	.01	.0007	.0003
No Missing Codes (Bits)	12	14	16	16	16	16	20	16	18	12	16	20
THD (%)	.008	.003	.001	.001	.001	.007	.0003	.0015	.0015	.02	-	-
Dynamic Range (dB)	73	83	92	92	92	84	120	95	98.5	70	-	-
Power Dissipation (mW)	120	120	120	280	40	220	150	450	450	750	25	25
On - Chip S. & H.	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
On-Chip Filtering	-	-	-	-	-	YES	YES	YES	YES	-	YES	YES

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ELECTRONICS NEWSLETTER

CRAY COMPUTER'S FIRST PRODUCT: A SOUPED-UP CRAY-2

Seymour Cray's GaAs-based Cray-3 supercomputer may be just around the corner, with first deliveries now expected in 1991. But there's still some life left in the old, silicon-based Cray-2 architecture. Cray Research Inc. of Minneapolis is building a special, eight-processor version of the four-year-old machine, doubling the number of processors and boosting performance to the level of the high-end Cray Y-MP. If all goes as expected, it will be marketed by Cray Computer Corp., the Colorado Springs subsidiary that Cray Research plans to spin off as a separate company by year's end, subject to Internal Revenue Service approval [*Electronics*, June 1989, p. 30]. Seymour Cray will head the new firm and take over the risky Cray-3 project. By providing the startup with a product to sell now, the souped-up Cray-2 will make Cray Computer "a going concern," says one Colorado executive. That status will help Cray Computer meet IRS requirements. The machine is expected to be ready for shipment early next year. ☐

COMING SOON: 40-GHz SILICON BIPOLAR TECHNOLOGY

Tokyo's NEC Corp. has devised the speediest silicon bipolar LSI technology yet: its device runs at a blazing 40 GHz with an ECL gate-delay time of a mere 29 ps. The NEC process will be unveiled at the International Electron Devices Meeting, beginning Dec. 3 in Washington. Other highlights among the 200 papers slated for IEDM are a 0.5-μm biCMOS technology from Texas Instruments for logic and 4-Mbit SRAMs (its six-transistor SRAM cell is only 23 μm^2); a GaAs VLSI 16-by-16 multiplier chip from Honeywell with 4,500 logic gates and 22,000 FETs, a record for GaAs; and tunable semiconductor lasers from Bellcore capable of wavelength switching and data modulation of up to 20 AM or 48 FM channels at 200 Mbits/s. This will make possible multiwavelength packet switching in lightwave networks. ☐

SKY'S ACCELERATOR MARRIES INTEL'S i860 AND i960 PROCESSORS

It looks like the first product to harness the dual power of Intel Corp.'s RISC-based i860 and i960 CA microprocessors will be an application-accelerator board scheduled for introduction next month by Sky Computers Inc. of Chelmsford, Mass. The board aims to boost the performance of Sun Microsystems Inc. work stations and other VMEbus-based platforms used in scientific and engineering applications, including simulation, computational fluid dynamics, and 3-d visualization. Sky will apply the i960 CA superscalar device as an I/O processor, offloading the i860 CPU from those tasks. Sky isn't talking yet about how fast the board will be, but the i960 CA is rated at 66 mips in scalar operations and the i860 combines graphics and floating-point capabilities on one chip. ☐

COGNEX BROADENS ITS MACHINE-VISION BASE IN JAPAN

A Needham, Mass., manufacturer has formed its third major Japanese alliance in a year to provide machine-vision systems for use in Japan. Cognex Corp. has just linked with Komatsu Ltd., a Tokyo-based provider of industrial equipment, in a four-year "multimillion-dollar" contract for machine-vision systems that Komatsu will use, among other things, for factory automation. Komatsu will add Japanese user interfaces and ruggedize the units for industrial settings. Cognex is already delivering machine-vision systems to Shinkawa Ltd., a Tokyo supplier of semiconductor equipment, under terms of an earlier $9 million award—said to be the largest OEM machine-vision contract to date—and to Tokyo Seimitsu Ltd., which is using them for wafer alignment in an automated wafer-dicing machine. ☐

ELECTRONICS NEWSLETTER

NATIONAL'S TAPEPAK TAB SYSTEM WINS TWO CONVERTS

National Semiconductor Corp.'s advanced surface-mount packaging system using tape-automated-bonding technology taken another step toward becoming a de facto standard in high-density VLSI packaging. Northern Telecom Inc. of Nashville, Tenn., and Advanced Micro Devices Inc. of Sunnyvale, Calif., have adopted the TapePak system, which uses a molded, gull-wing package built around chips bonded to a copper tape [*Electronics,* Feb. 18, 1988, p. 104]. Packages can house devices with up to 576 leads with pitches as small as 0.25 mm for metric packages and 10 mil for nonmetric packages. Using TapePak, package size can be reduced to between one-third and one-tenth that offered by conventional packaging techniques. □

HERE'S A SWITCH: TI BUYS TECHNOLOGY—FOR HDTV—FROM JAPAN

Bucking tradition as well as prevailing theories about U. S.-Japan technology flow, Texas Instruments Inc. has agreed to purchase basic semiconductor technology for high-definition TV from Japan. The sellers will be that country's public TV broadcasting entity, Nippon Hoso Kyokai (NHK), and a group of companies. Dallas-based TI, with its strong patent position, has usually sold its technology or the right to use it; the Japanese, on the other hand, have been accused of refusing to transfer chip technology to non-Japanese firms. Initially, TI Japan will develop chips for the Hi-Vision, or MUSE, HDTV receiver market in Japan. However, it expects to have a line of circuits that meet the standards for all three markets: MUSE in Japan, HD-MAC in Europe, and any future U. S. standard. □

CONVEX OPENS ITS MACHINES TO USE AS CENTRAL COMPUTERS

Minisupercomputer leader Convex Computer Corp. is unveiling several software and hardware upgrades for its C Series systems this month as part of a package the company calls Open Supercomputing. Besides making Convex machines open and easier to use in heterogeneous computing environments, the moves by the Richardson, Texas, company are aimed at encouraging use of Convex as a central computing resource. Until now, Convex systems, which sell for up to $2.5 million, have been used largely for departmental supercomputing. To support large corporate data bases, the firm is rolling out a high-performance disk subsystem called the Integrated Disk Channel that can support up to 32 high-speed IPI-2 (for Intelligent Peripheral Interface) disk drives. With the IDC, Convex claims the highest packaging density in the industry—16 Gbytes per 6.5 ft^2 footprint—as well as sustained data-transfer rates of 20 Mbytes/s. Another hardware addition boosts scalar performance on Convex machines typically by 20% for vector/scalar codes with a heavy scalar content. □

DEC'S MULTI-CHIP PACKAGING TOPS PC-BOARD DENSITIES

Providing a rare peek into its research and development strength, Digital Equipment Corp. of Maynard, Mass., has unveiled a multifaceted method for packaging semiconductors that can handle device densities up to 30 times greater than conventional printed-circuit boards. A copper and polyimide High-Density Signal Carrier offering nine layers for power and signal use replaces a pc board. Sophisticated lithography allows it to carry very dense packages because it offers typical line widths of 15 µm with 60-µm spacing. That means typical propagation delays between chips of 160 ps/in. The HDSC and its devices are mounted to a Multi-Chip Unit, which holds as many as 72 VLSI devices. Flexible signal connectors link the HDSC to a Planar Module, carrying up to 800 signal paths per unit. □

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NEWS UPDATE

Entry Price Redefined for Hardware Accelerators

The industry's lowest prices for logic and fault simulation accelerators have been announced by Zycad Corporation. Bundled as a complete system, the Magnum™ Series of simulation accelerators delivers 16,000 gate modeling capacity, serial fault simulation, and ZILOS™ software interface for $55,000.

One Million Gate Barrier Broken

Large system designs of up to four million gates can now benefit from the performance of hardware acceleration. Zycad's System Evaluator™ combines 128 custom, parallel processors to produce 320 million event per second simulation speeds. Over 6,000 times faster than simulations running on 10 MIP workstations, the SE makes virtual prototyping of entire computer systems a reality.

Behavioral Simulation Speed Triples for Accelerator

Behavioral simulation speed has been increased for Zycad's MACH™ Series hardware accelerators. The MACH 1500™, with its new UNIX™ front-end processor, performs logic and fault simulation two to three times faster than previous models. Integration of the processor with the simulation acceleration hardware ensures that added processing performance translate directly into faster simulations. Total simulation throughput, including netlist compilation and output processing, also benefits from increased processing performance. MACH accelerators are available from only $60,000.

Fault Simulator Sets Speed and Capacity Record

One million gate designs can now be fault simulated on Zycad's MACH 2000™ hardware accelerator. A new parallel-concurrent fault simulation algorithm increases the accelerator performance by processing up to 64,000 faults in a single simulation pass. A new front end processor delivers 10 MIPS of behavioral-level simulation, netlist compilation and output processing performance.

VHDL Simulator Solves Complex Problems

Zycad's System VHDL™ simulator, a full implementation of the IEEE 1076 standard, is now in use for the verification of complex designs. From analyzing the design of military computers to verifying the correctness of synthesized logic, this new simulator has demonstrated the speed, power and capabilities of the Zycad VHDL product. The industry's first VHDL source-level debugger comes standard with the Zycad System VHDL. The state of simulation variables is displayed as each line of VHDL code is executed, thus simplifying the development and verification process. Zycad System VHDL is available now and runs on Apollo™ and Sun™ workstations, and VAX™ computers.

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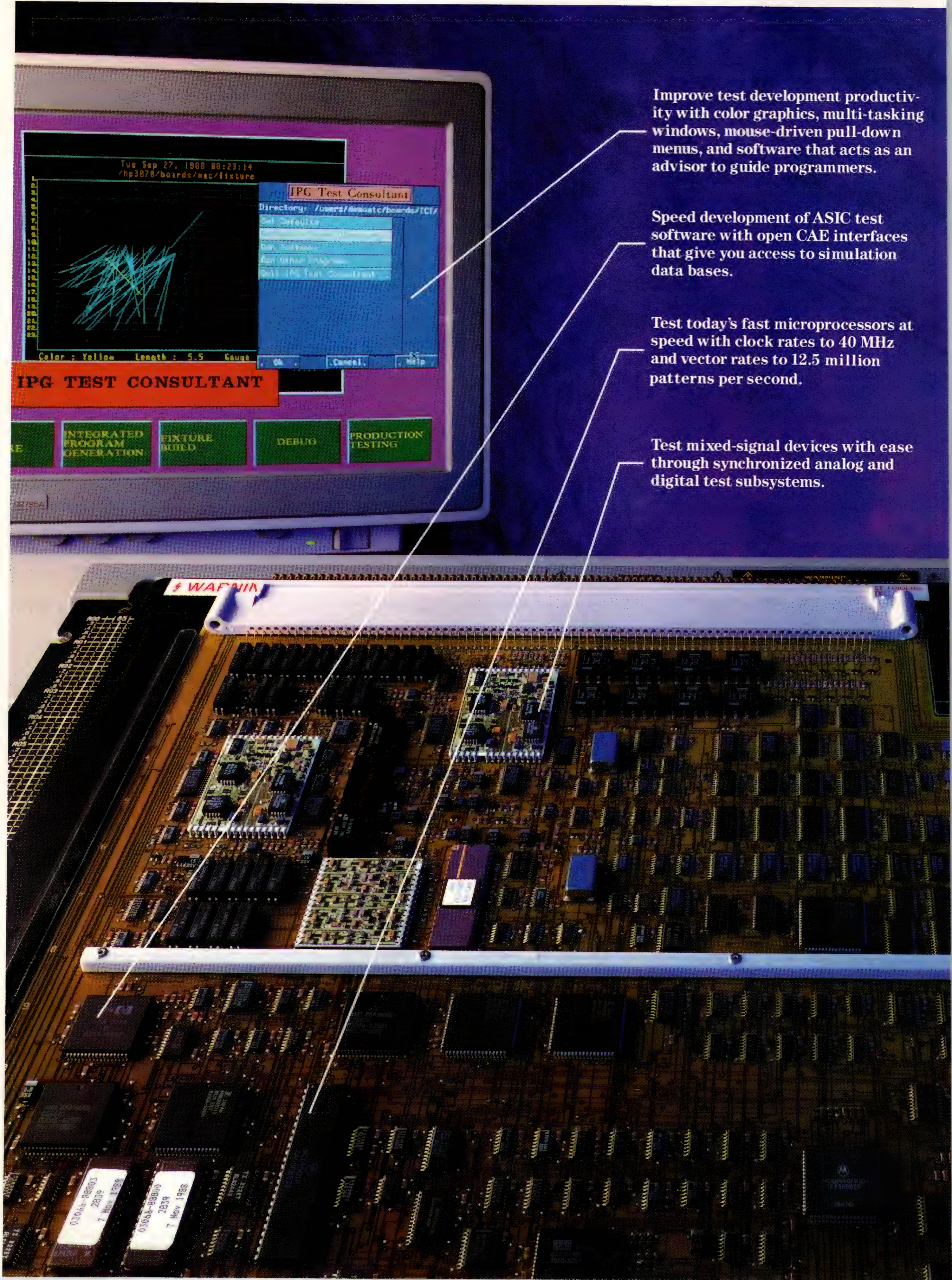

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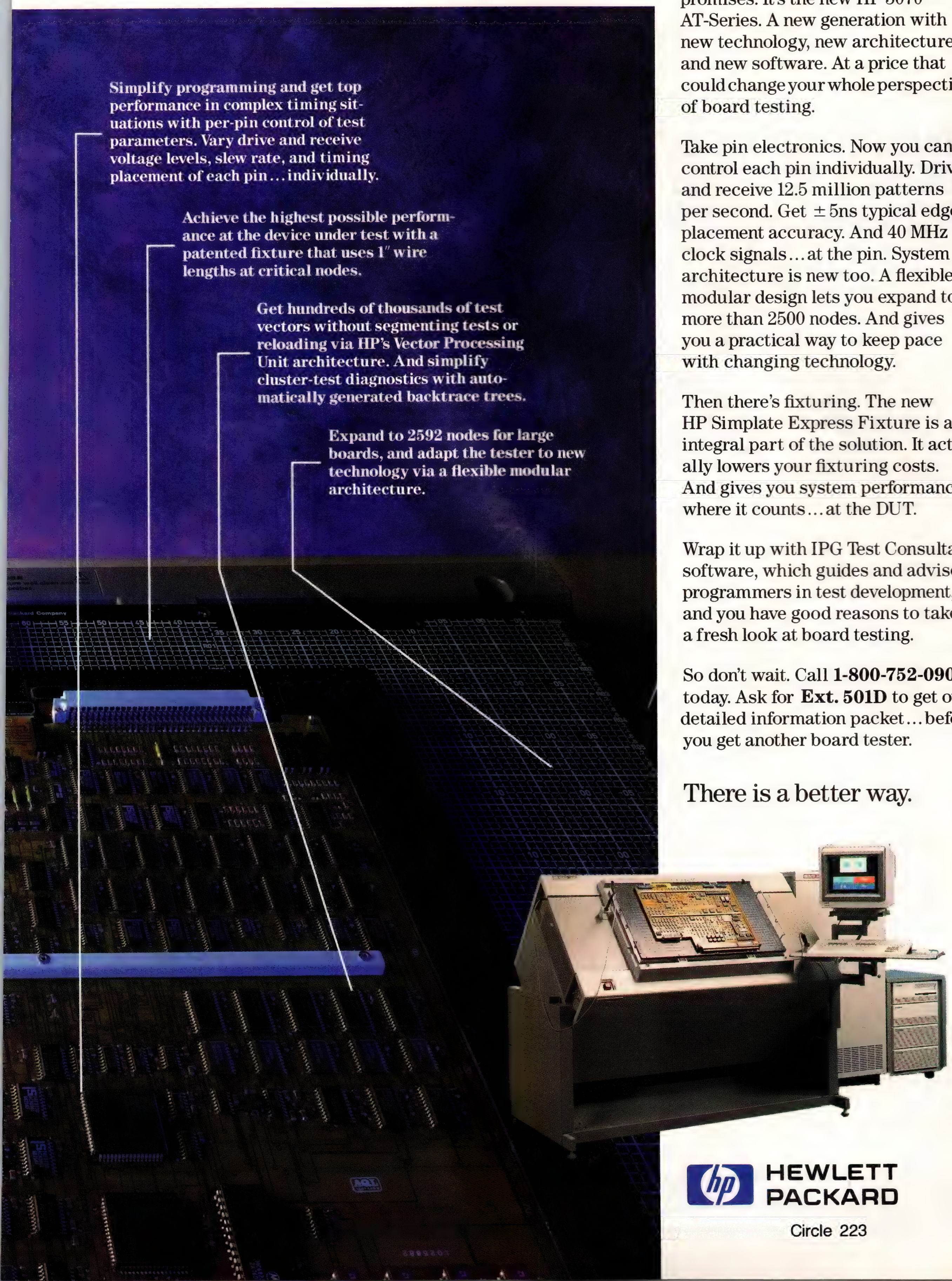

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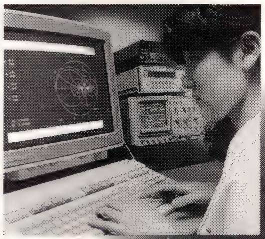


Using CAD, a high-frequency circuit is simulated under various conditions.
Good components can only be produced by using good materials and optimum design.

TALKING ABOUT DIGITAL COMMUNICATIONS WITH ANALOG COMPONENTS.

Continuous technological inovations for ever changing Market needs. — Murata.

Today, highly-sophisticated information communications systems, such as satellite communications, satellite broadcasting, and mobile communications, are indispensable. The digital transmission of more information more accurately and speedily is supported by MURATA's analog circuit technology. Mr. Toshio Nishikawa, a director of Murata having many years of experience in communications technology, discussed Murata's role.

Q: What is the relationship between high frequency signal transfer and digital transmission systems?

A: Highly-sophisticated information communications systems which transmit digital information, such as ISDN, are being established. Since the assigned wave band for wireless communications has become narrower, it is necessary to increase the frequency of the carrier wave. A digital signal is confined to the high-frequency analog signal which acts as this carrier. Thus, analog circuit technology for transmitting a digital signal without distortion is required for a high-frequency signal transfer.
To obtain an accurate digital signal, high-performance and high-frequency analog components are required.

Q: What action is MURATA taking?

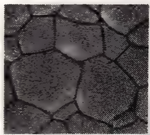
A: To select without distortion, waves according to the frequency bands required by customers, MURATA is marketing various types of microwave filters.
This was realized by developing unique dielectric ceramic materials exhibiting excellent dielectric constants, Q values, and temperature coefficients.

Q: Is MURATA developing other materials?

A: Yes. MURATA is setting up a system for its own integrated development and production of related parts, such as electrode materials, including silver-palladium electrode, alumina substrates, and chip monolithic ceramic capacitors.

Q: What is special about MURATA besides the filter?

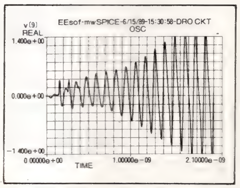
A: Included in our product line is an oscillator produced from the idea that the integration of components produces new functions. To obtain very high stability in the oscillator, MURATA is using a dielectric resonator. This resonator maintains ±10ppm or less in frequency variations in a 12-year life test. We are highly confident that our company owes its results to the completed material technology, mechanism design technology represented by the high-frequency coaxial connector, circuit design technology realizing a high function, using CAD, and its uniquely developed evaluation technology.



Microscopic photo of dielectric ceramic crystal surface: particles are closely arranged in order.

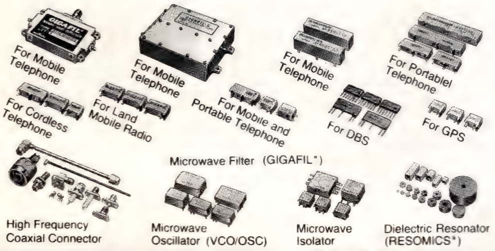
Q: Last, what is MURATA's future theme?

A: Since the size of the component is reduced as the frequency becomes higher, more highly sophisticated technology is required. It is necessary to make materials finer, the components themselves more accurate, and to fully arrange circuit and measurement technologies.
MURATA intends to contribute to the development of a highly sophisticated information-oriented society by developing more functional components.



Simulation of startup waveform after the microwave oscillator supply voltage is applied: a steep startup is required for an oscillator.

Smith chart and digital signal: MURATA components reliably transmit digital signals confined in analog signals. We accurately determine high-frequency characteristics by using the Smith chart.



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PRODUCTS TO WATCH

DIGITALK BRINGS OBJECT-ORIENTED PROGRAMMING TO PRESENTATION MANAGER

The snail's pace of application development for Microsoft Corp.'s OS/2 and Presentation Manager is likely to speed up thanks to an object-oriented-programming development environment from Digitalk Inc. The Los Angeles company's Smalltalk/V PM represents a major restructuring of its Smalltalk environment for the MS-DOS and Macintosh operating systems. The object-oriented concepts of encapsulation and inheritance provide easy-to-maintain and reusable code at no sacrifice of performance. Using Smalltalk/V PM, the developer also has complete access to Presentation Manager features such as Dynamic Data Exchange and Dynamic Link Libraries, both of which make it easier to pass data to and from Presentation Manager tools and other applications. Available now, Smalltalk/V PM is priced at $500 and includes a tutorial on object-oriented programming. □

ZILOG ROLLS OUT FOUR Z80 SPECIAL-PURPOSE CHIPS

New from Zilog Inc. is a range of devices based on the Campbell, Calif., company's Super-Integration standard cells. The 8-bit Z80 gets four higher-integration follow-ons and a family of data communications controllers. In the first category are the Z84013/84C13, which incorporate serial input/output and a counter-timer, and the Z84015/84C15, which add parallel I/O and other features, including power-on reset, two chip-select pins, and error-detection circuitry. For datacom, the company's Z16C35 features a programmable bus architecture, four direct-memory-access controllers, and a 50% higher data-transfer rate of 3 Mbits/s. The Z16C33, a monochannel universal serial controller, features time-slot assignment support of synchronous data-link control. Pricing is $11 to $13 each for the processors and $20 to $25 each for the datacom chips. □

FLANDERS'S CONTROLLER CARD SETS THE PACE FOR PRINTING, IMAGE RETRIEVAL

Systems integrators and original-equipment manufacturers specializing in high-resolution desktop-publishing and image-retrieval systems can now boost printing speeds up to 10 times and gain access to other enhanced performance features. The Exact-2000 controller card from Flanders Research Inc. delivers 1,600-by-1,200-pixel resolution, scalable printer and screen fonts, and compatibility with Postscript software fonts. Plugged into a standard PC AT slot, the card achieves its speed and graphical manipulation marvels by using proprietary code to implement Microsoft Windows' Graphical Display Interface. The card features built-in compression/decompression, which means that only compressed images travel across the host bus or reside in the host's memory. Priced at $1,900, the Exact-2000 complements the Flanders, N. J., company's $2,500 Exact-2000 monitor. □

TADPOLE CLIMBS ONTO THE INTEL i960 RISC BANDWAGON

Tadpole Technology Inc. will add Intel's i960 CA reduced-instruction-set-computer microprocessor to its repertoire of RISC engines for its single-board-computer product line. The Waltham, Mass., company already has a Motorola 88000-based RISC board [*Electronics,* July 1989, p. 23]. Its i960 CA-based TP960V will come in three variations using either 20- or 33-MHz versions of the 66-mips chip. Intended for use in embedded real-time systems, the board can be tailored to customer needs and is expected to include provisions for the SCSI interface, Ethernet, serial input/output, and EPROM as standard. To be available late this year, the lowest-speed version is priced at about $3,000 in volume. The board competes with the HK80/960E from Heurikon Corp., Madison, Wis. □

PRODUCTS TO WATCH

PC CHIP-SET FRATERNITY HERALDS NEW ARRIVALS FOR LAPTOPS . . .

Activity in the IBM PC chip-set market remains frantic. On the heels of last month's unveiling of Zymos Corp.'s System 90, a chip-set family for the Intel Corp. 80386SX and 80486 processors, another Sunnyvale, Calif., chip maker is about to jump into the fray. Oak Technology Inc.'s Oak Horizon chip set, targeted for use in 80286 and 80386SX laptops, includes a system controller, an input/output peripheral controller, a direct-memory-access and memory controller, a buffer and real-time clock, and a data-buffer and power manager. The Oak Horizon costs $90 a set in 1,000-unit quantities. The first member of Zymos's new chip-set family, System 90/SX, features a peripheral coprocessor, an intelligent look-ahead memory coprocessor, a high-performance bus interface, and a local-bus gateway chip. System 90/SX is available in 16- and 20-MHz versions and costs $115.35 each in 100-piece quantities. □

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The first numerics coprocessor that's fully compatible with Intel Corp.'s floating-point coprocessor for the 80386 provides 10 times the power of standard math processors, according to its developer. Designed for IBM PCs or any system with a slot that accepts Intel's floating-point coprocessor for the 80386, the 83D86 FasMath processor from Cyrix Corp. delivers 5.5 million floating-point operations per second. The Richardson, Texas, company's chip is available in 20-, 25-, and 33-MHz versions. In 100-piece quantities, the 83D86 is priced at $471, $585, and $773, respectively. □

AUSPEX'S UNIX NETWORK SERVER BOASTS A TENFOLD I/O EDGE

By using large, directly addressable primary-data-cache memory and by separating the Unix operating system from the file system, Auspex Corp. claims that it has boosted the input/output capacity of its Unix network server to 10 times that of conventional server architectures. In the Sun Microsystems Inc. environment, the NS 5000 can process 1,000 Network File System operations per second, claims Auspex, which is based in Santa Clara, Calif. The server connects as many as eight Ethernet local-area networks, providing a total I/O capacity of 80 Mbits/s. Because it can handle that many Ethernet LANs, the server eliminates the need for routers to be inserted between segments. Similarly, redundant copies of shared applications, libraries, and data can be kept to a minimum. The NS 5000, slated to be available in January, will cost about $115,000. □

CSP SPEEDS UP ITS ARRAY-PROCESSOR BOARDS WITH INTEL'S i860

CSP Inc. is putting Intel Corp.'s i860 on its boards in an all-out bid to take the lead in the array-processor add-on market. The Billerica, Mass., company's SC-1 (for SuperCard-1), the first in a promised family of products, uses the 33-MHz, 66-megaflops version of Intel's RISC chip. The SC-1 can perform a 1,024-point complex fast Fourier transform with bit reversal in 0.96 ms; the previous best for a CSP board for that operation was 1.4 ms. FFTs are typical tasks for array processors, which allow more extensive programming to customize boards than do application accelerator boards. Applications for the SC family include signal, image, and seismic processing. Some 550 applications in the CSP software subroutine library run on the SC family. The SC-1, scheduled to ship in December, will initially support the VMEbus only, but CSP promises versions for PC AT and EISA buses. A version with 2 Mbytes of memory will sell in single-unit quantities for $7,995. An 8-Mbyte array processor will cost $10,995. □

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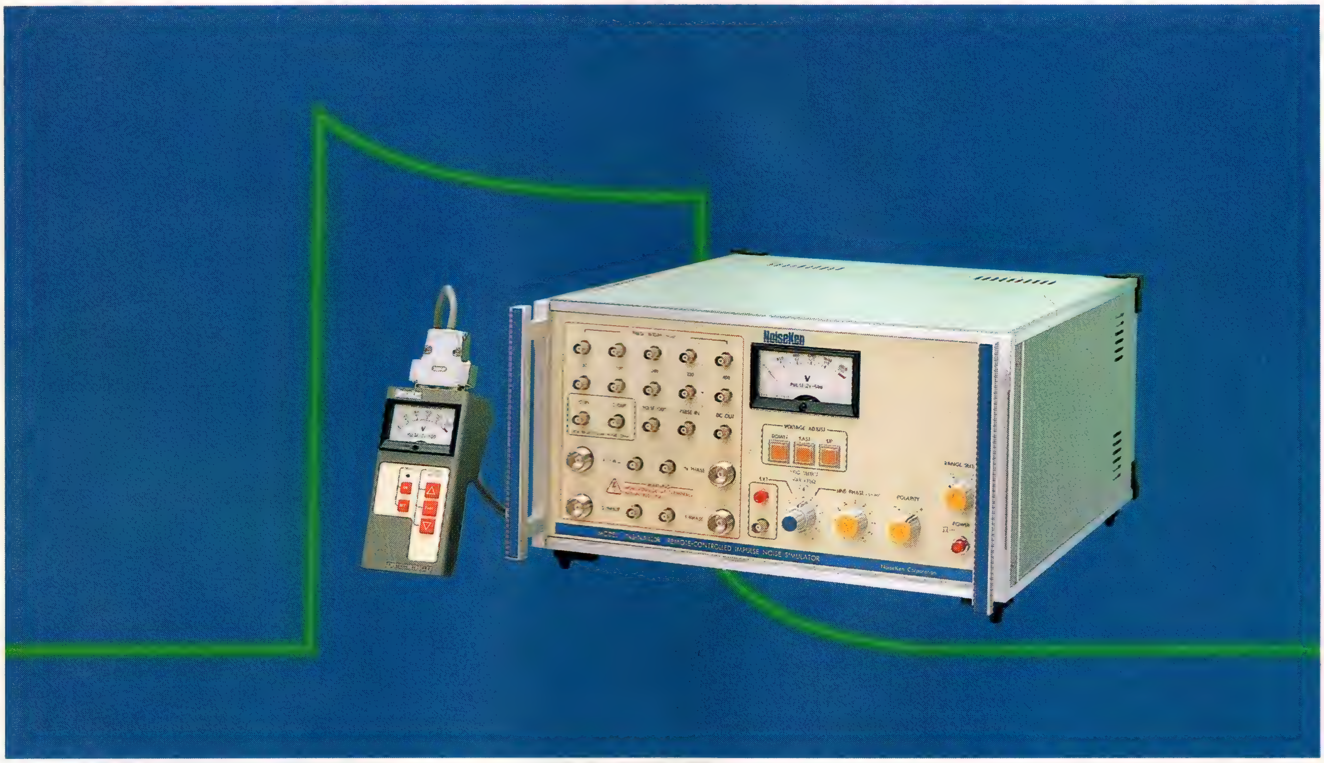

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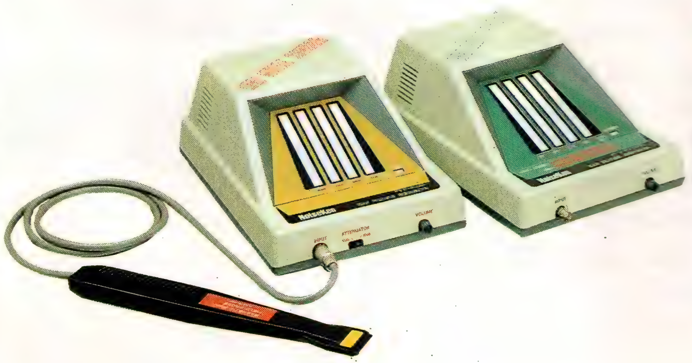

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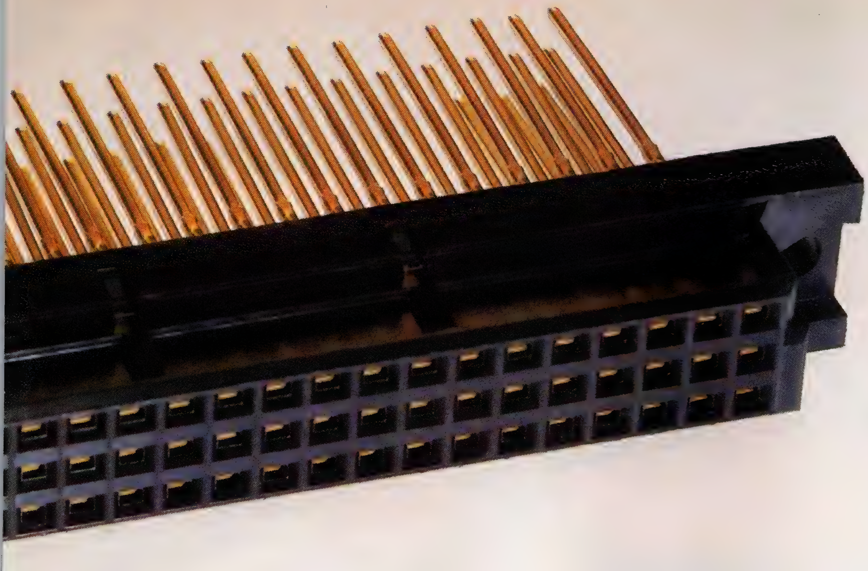

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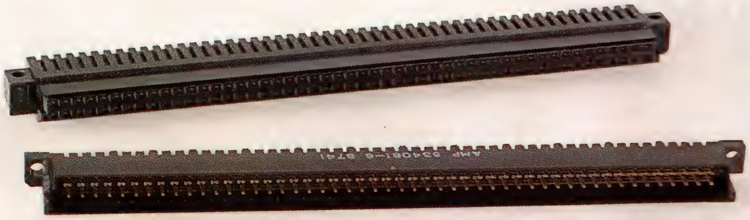

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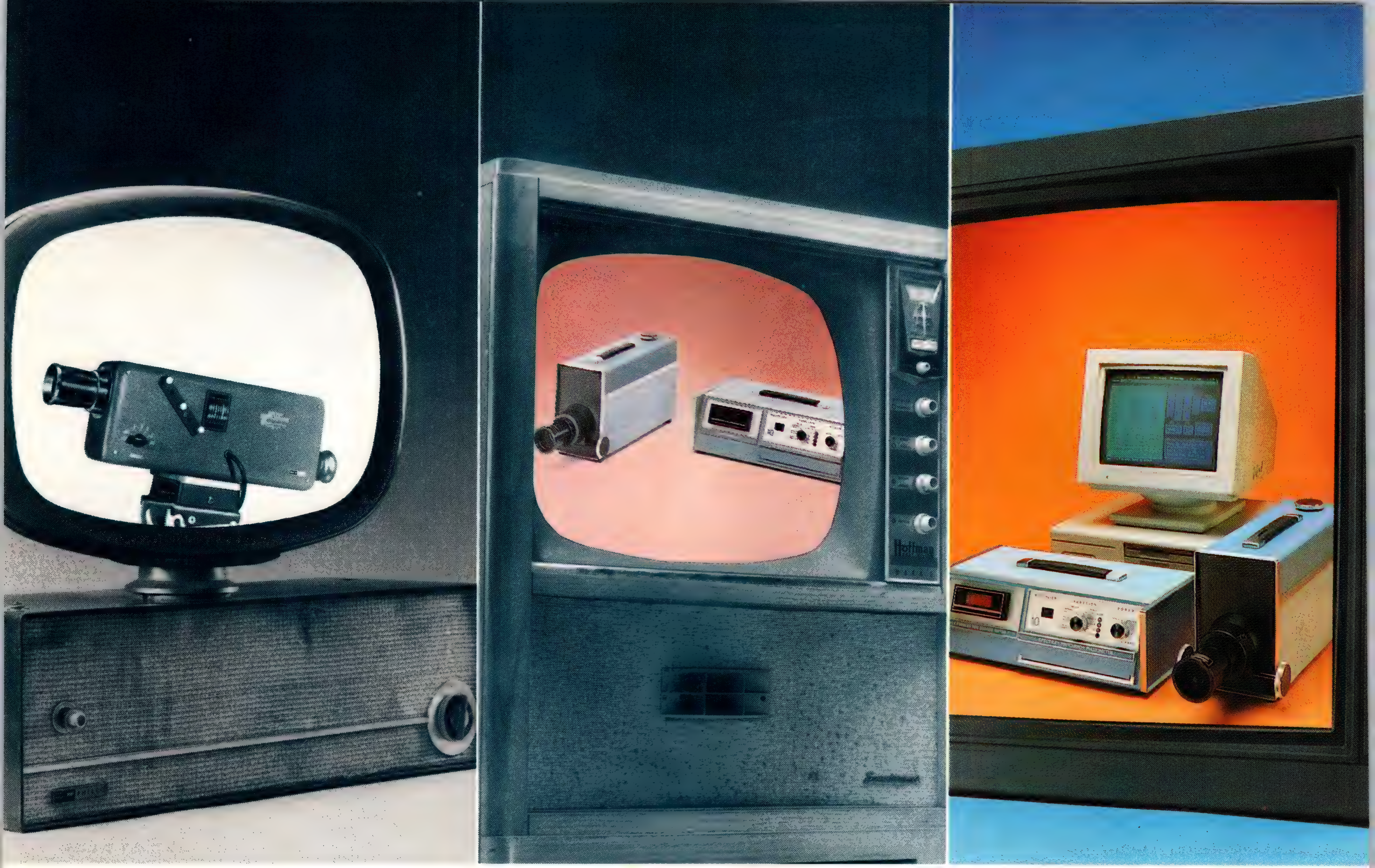

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THE STAKES ARE GETTING HIGHER IN EMBEDDED CONTROL

Intel and others debut chips aimed squarely at Motorola's turf

SAN JOSE, CALIF.

In the fast-paced poker game of 32-bit embedded processors, Motorola Inc. holds the hottest hand and the most winnings in a market that is expected to ship 28 million units by 1993. But now other players are anteing up big bucks to try to win some of Motorola's booty, even as the market itself undergoes a sea change.

With office peripherals starting to edge out system central processing units as the dominant sales target, a handful of companies are chasing down the market leader. They are Advanced Micro Devices, Cypress Semiconductor, Inmos, Integrated Device Technology, Intel, National Semiconductor, and VLSI Technology. Three of them tossed new chips into the pot last month, as did Motorola.

Aimed at jobs where the need is for high computing power is the i960 CA, a reduced-instruction-set chip rated at a sizzling 66 million instructions per second. It comes from Intel Corp.'s Microcomputer Division in Chandler, Ariz.

Two other devices promise lower system cost with enough processing power for large-volume imaging applications. They are the 20-mips IMS T400 from Inmos Ltd., a member of the SGS-Thomson Microelectronics Group based in Bristol, England, and the VL86C020 from VLSI Technology Inc. of Tempe, Ariz.

Motorola, meanwhile, weighs in with the 68302. Aimed at communications applications, the chip supports five major communications protocols, including the integrated services digital network and the High Level Data Link Control. The company, whose 68020 is designed into most of today's laser printers, is wagering on a three-pronged strategy to head off the competition. It plans to add to the 68000 family, develop devices such as the 68302 in the more integrated 68300 family, and target the 88000 for high-end embedded-processor applications.

DIFFERENT GAME. Adding zest to the action is the complexion of the market, which is distinctly different from the general-purpose microprocessor arena. Embedded processors are price-sensitive and thus have small chip counts, says industry watcher Michael Slater, editor and publisher of the *Microprocessor Report*, a Palo Alto, Calif., newsletter. What's more, he says, they have relatively small amounts of program code compared with general-purpose devices and have no brand-name recognition.

As a result, embedded-processor sales have tended to trail those of their general-purpose cousins. Five years ago, the bulk of 16-bit microprocessors were shipped for general-purpose applications. Today, 60% of them are in embedded applications, says Steve Goldstein, director of marketing at Ross Technology Inc., the Cypress subsidiary in Austin, Texas.

Complicating matters is a basic change in the way 32-bit embedded processors are going to be used, with office equipment replacing system CPUs as the dominant end product. In 1988, 64% of the 4.3 million 32-bit microprocessors shipped wound up as system CPUs, reports market researcher Dataquest Inc. of San Jose, with 21% going into embedded applications in office equipment. But in 1993, says Dataquest, just 26% of the 28 million units shipped will be for system CPUs and 52% will be used in office systems. (The remainder of the market is made up of processors aimed at communications and other equipment.)

Office equipment is replacing system CPUs as the dominant end product

The imaging component of the office market will soon pass mass storage in use. Laser printers, X-Windows terminals, scanners, faxes, and color laser printers are all candidates for embedded control. Dataquest puts 1988's usage at 14,000 units for imaging and 76,000 for mass-storage office products. The 1993 totals will be 13.3 million for imaging and 1.6 million for mass storage, the research group predicts.

As a result, makers of embedded processors are spending more time at the office. National Semiconductor Corp., for one, is concentrating on this area with its latest 32CG16 and 32CX32 chips. Aimed at office imaging work, these parts contain hardware and software hooks in the core, especially for tasks such as fast-block-move operations.

Intel's breakthrough with the i960 CA is the device's ability to execute more than one instruction per clock cycle. The chip's designers accomplish this with multiple instruction units and a pipelined architecture sporting a 128-bit-wide instruction cache, says Alan Steinberg, marketing manager for the i960 product family. The cache feeds four instructions into on-chip multiple-instruction execution units at once. "Instead of a higher clock rate, you get multiple mips by doing more integer operations per cycle," Steinberg says. "It is the first [architecture] of its kind to do so."

As a result, the Intel device doesn't drive the clock frequency beyond 33 MHz. A higher frequency would mean faster, more expensive peripheral chips and memory elements to complete a system.

The Intel approach has caused competitors to sit up and take notice. Advanced Micro Devices Inc. of Sunnyvale, Calif., is working on a chip that can likewise perform pipelined multiple instructions in one cycle, says industry watcher Slater. And a new National part, to be introduced next year, will employ pipelining for executing multiple instructions per clock and higher levels of integration, says Russ Johnson, director of the Santa Clara, Calif., company's imaging group. The new design will be implemented in a 1.0-μm CMOS process, scalable to submicron technology, Johnson says.

LOST COUNTS. For all the vendors, the main concern is cost, says Goldstein of Ross Technology. The conundrum for the Intels, Motorolas, and AMDs with their dedicated RISC processors for embedded applications is that other RISC chip makers are trying to win designs from Motorola based on a lower total system cost. That's where the new contestants—Inmos and VLSI Technology—come in. Priced at $20 and rated at 20 mips, the Inmos IMS T400 sets a new low in price/performance for an embedded RISC processor, Inmos says. VLSI's VL86C020, an enhanced version of its VL86C010, runs at 15 mips.

The trend in these low-cost offerings is to incorporate functions on-chip that reduce the system cost yet maintain a performance edge over the ubiquitous Motorola 68000 family. Inmos, for example, has incorporated a dynamic random-access-memory controller on the T400 as well as support for up to 16 Mbytes of static column DRAM.

RISC processor suppliers such as Cypress Semiconductor Corp. of San Jose are promoting the flexibility of their solutions. With Cypress's Sparc-based CY7C601 processor and associated peripheral chips, the designer selects only the firepower needed. For example, the chip set contains a memory-management unit and floating-point coprocessor. If those functions are unneeded, the user does not pay extra for those chips. Like Cypress, Integrated Device Technology Inc. of Santa Clara is betting that its MIPS-based 79R3000 RISC processor and peripheral chips also have a chance of winning some of Motorola's share.

Motorola's response to the competitive threat will go in two directions. "First, customers will want to migrate to faster, higher-performance 680X0 chips—the 020, 030, and 040—to achieve higher page-per-minute performance," says Brian Wilkie, advanced microcomputer product manager for Motorola in Phoenix.

"The other direction is toward lower cost by integrating more functions around a 68000 core, via the 68300 family of chips," he says. Motorola professes to be unconcerned about the onslaught of high-performance chips coming onto the market that are aimed at the high end. "Our strategy is to use the 88000 as an embedded processor in this high-end arena," says Wilkie. *–Jonah McLeod*

HDTV

DIGITIZED HDTV TURNS UP THE HEAT

OTTAWA, CANADA

As the first North American version of high-definition TV gets ready for its debut in Canada next month, forces are aleady coalescing that may fundamentally alter HDTV by the time of its full-scale U. S. deployment in the mid-1990s. Although the Canadian trial involves an analog transmission system, digital HDTV is making a strong bid for domination in the U. S. Technology options are only part of the story; the outcome of the technology tug of war is likely to determine who will lead the broadcast industry into the next century.

If the phone companies, computer makers, and over-the-air TV broadcasters have their way, HDTV in the U. S. will be digital. Phone companies, which hope to some day gain permission to distribute TV programming, need a digital signal that is compatible with their switching infrastructure. Computer makers are behind digital technology because it is much easier to combine digitized video with other media for integration into multimedia schemes now showing up in the marketplace [*Electronics*, May 1989, p. 42].

For over-the-air TV broadcasters, digital transmission offers a way to make the most of precious bandwidth. Digitized video can be compressed to a greater extent than analog signals. "Broadcasters are interested because their media—the ether—gives them a very, very small available bandwidth," says C. A. A. J. Greebe, director of electronic systems research at North American Philips Corp. and head of Philips's HDTV U. S. research in Briarcliff Manor, N. Y.

One leading video-conferencing company—Compression Labs Inc. of San Jose, Calif.—has teamed up with the Tokyo Electric Power Co. to develop a codec that digitizes HDTV (see p. 87). "We are convinced we can put full-featured HDTV—full-motion, 30-frame/s video with stereo audio—on a 44-Mbit/s fiber pipe," says Todd Townsend, vice president for new product development at Compression Labs. "Some time ago, [Tokyo Electric] began bundling a fiber cable in its power-distribution lines. When it realized it had most of Tokyo wired, it formed a telephone company subsidiary."

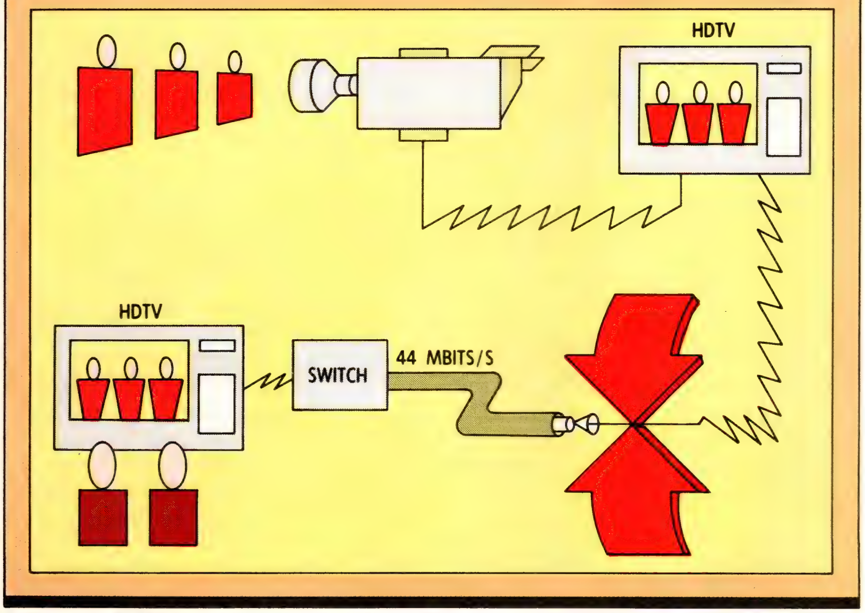
LOCKED OUT. In the U. S., telephone distribution is not so simple. The 1984 Cable TV Act prohibits phone companies from creating, programming, or marketing TV services, says John Wolfe, spokesman for the National Cable Television Association, a Washington-based trade group. The Modified Final Judgment that has governed phone company operations since the 1984 divestiture of AT&T Co. also bars phone companies from getting into the TV act, he says.

The cable TV industry is backing analog HDTV systems like the one scheduled to begin next month in Canada. Scientific Atlanta Inc. is set to deliver its closed-circuit HDB-MAC equipment to Telesat Canada in Ottawa. The HDB-MAC analog transmission system is based on very-small-aperture-satellite technology; it uses multiplexed analog component techniques and is an extension of Scientific Atlanta's B-MAC satellite delivery system, says John Messerschmitt, director of the Atlanta-based company's Advanced TV Systems Division.

Telesat Canada will use the system in a two-year trial to broadcast cultural and sporting events, as well as meetings, conferences, and special events. HDB-MAC is also one of 11 satellite-delivery HDTV systems to be tested for deployment in the U. S. by the Advanced TV Test Center in Alexandria, Va., early next year.

Not surprisingly, phone companies are working hard to remove the legal obstacles to their involvement in TV broadcast-

SQUEEZING HDTV FOR FIBER



To transmit HDTV signals over the 44-Mbit/s fiber cable in their trunk lines, phone companies need better compression technology—and permission from Congress and the courts.

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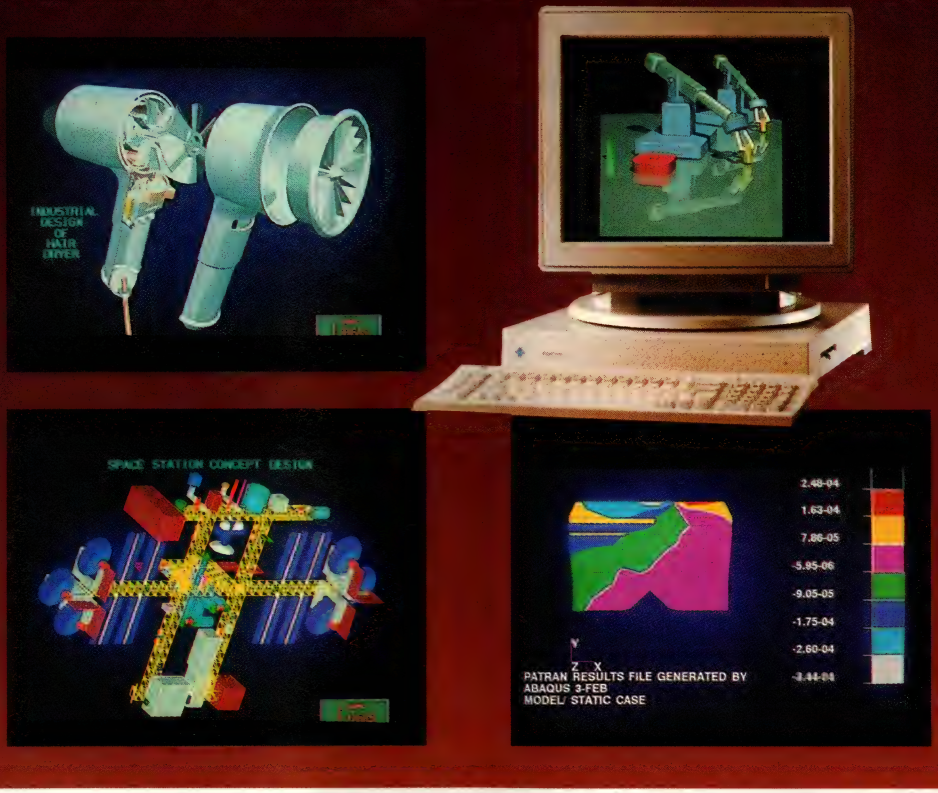
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ing. Deployment of fiber in the local loop has been getting cheaper and will cost about as much as conventional copper lines in the early 1990s, says John Sodolski, president of the Washington-based U. S. Telephone Association. The deployment of fiber would accelerate if phone companies have the incentive of a lucrative market such as delivering TV signals, he asserts. "If we are allowed to send TV programming, by 1995–97 a significant part of urban America will be served by fiber, and in 12 years, a significant part of *all* of America will be served," Sodolski says. The telephone association supports pending legislation in Congress that would allow Bell operating companies to include information and entertainment among their offerings.

Also not surprisingly, cable TV carriers are intent on making sure the telephone companies stay out of their business. "We heard a lot of noise from the phone companies about a year ago about getting into the TV business," says Wolfe. "But when people saw what they were really about, interest died." Although phone companies are pushing fiber as "the technology of the future," he says, their real interest is in making money.

Meanwhile, cable companies are starting to replace existing coaxial cable in neighborhood-to-neighborhood trunks with fiber. "As we upgrade the plant in bandwidth, we can save money [because the cost of fiber cable has dropped] and improve picture quality at the same time," says Dave Pangrac, director of engineering and technology at American Television and Communications Corp. Although the Stamford, Conn., cable TV company is a fiber proponent, it has no plans to install fiber in the local loop. Coaxial cable, which carries an analog signal very well, has all the bandwidth needed for HDTV, Pangrac says.

Telephone companies are promoting digital HDTV simply because it is compatible with digital switched networks, Pangrac says. Digitized signals, he contends, will not be user friendly. "Because of bandwidth limitations, you can pick up only three channels at a time. In a broadband analog system, you can have up to 14 sets in your house tuned to a different channel," he says.

MAJOR TOPIC. Bandwidth has become a major topic of discussion among companies eyeing digital HDTV. "One transmission rate for HDTV that is being discussed as a standard is 155 Mbits/s," says Philips's Greebe.

"A fair number of people think they can do 155 Mbits/s," says Compression Labs' Townsend. "That's a moderate level of compression. We've got some proprietary technology that makes us believe quite strongly that we can do it at 44 Mbits/s." From the phone company's point of view, 44 Mbits/s is the most attractive alternative because it is the most pervasive fiber-optic cabling.

Home delivery is much more sensitive to the bandwidth problem. "You have to be pretty good at compression to send in more than one channel on a single pipe," says Townsend. "More likely, there will be a switching scheme that delivers one channel but has a reverse channel for communicating back to the phone company. Customers would tell the phone company what channel they want. There are a lot of systems-level implications to doing that switching, but such systems have been built."

In the meantime, immediate and lucrative markets for digitized HDTV already exist. "The Defense Department has shown interest in promoting HDTV at levels as high as the Joint Chiefs of Staff," says Nick Arnett, Santa Clara, Calif.-based editor of *Multimedia Computing and Presentations.* The military is already the largest consumer of interactive video for training and simulations, one application that would be improved with HDTV systems. More important, says Arnett, is that HDTV accommodates large-screen, high-resolution monitors that show video and graphics. *–Jack Shandle*

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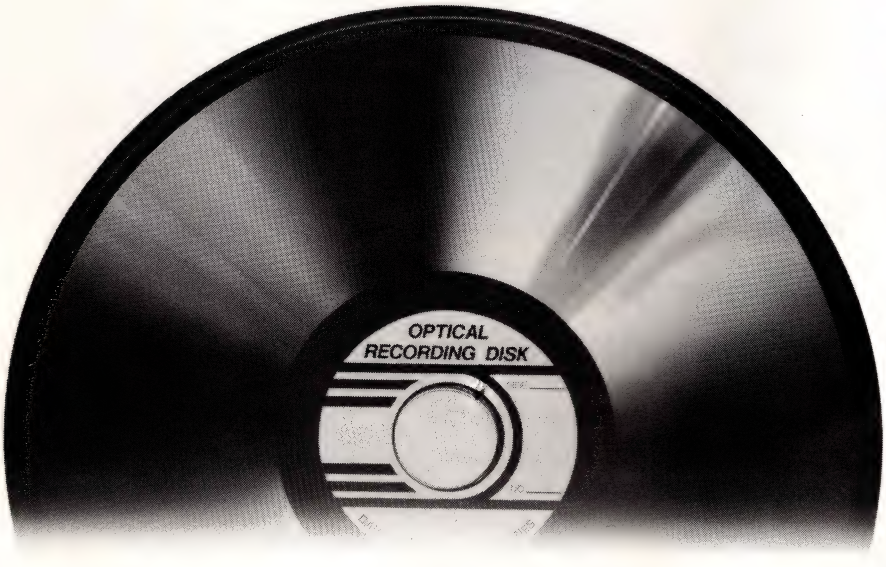

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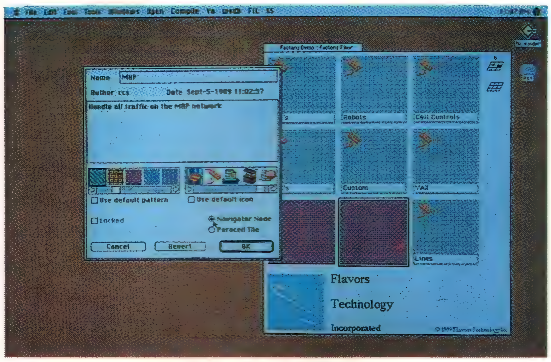
Circle 210

A SYSTEM WHERE THE LANGUAGE COMES FIRST

AMHERST, N. H.

Can Dick Morley do it again? Morley practically made modern automated manufacturing possible when he thought up the programmable logic controller 20 years ago. Now, as founder and chief executive officer of Flavors Technology Inc. in Amherst, he has come up with the Parallel Inference Machine, a system he describes as a real-time, rule-based systolic supercomputer, or rule server. Flavors says the PIM can execute 1 million rules per second in large parallel applications.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Flavors' programming language, Paracell, features the Navigator; it gives programmers a 3-d view of the data base.

The principal applications Morley has in mind are in aerospace and factory automation—areas faced with burgeoning needs for computing power and, says Morley, no practical way to meet them. The PIM could be the answer. For one thing, it can reliably host massively parallel applications. For another, it can dramatically reduce, at least conceptually, software programming time.

"There are two main thrusts of the architecture," Morley says. "One is a million rules per second, where the rules are relatively simple—expert systems have relatively simple rules. The other is rule-based programming. Most of the software guys acknowledge that rule-based programming is very productive—at least by a factor of 10 over classical programming. That makes large programs, such as in factory automation and Star Wars, much more realizable."

The architecture, however, is there only to play handmaiden to the expert-system-based language Paracell, which Morley developed for parallel processing. "I took the artificial intelligence concepts—all those things that deal with symbols. My symbols in this case are English words. I just wanted to make small, decomposable, independent chunks that talk to me in my language." Thus Paracell allows the programmer to render if-then-else statements in English or any other transliterable language—German, for example. Paracell has a vocabulary of structure-oriented words. "The structure is rather loose, but it's not informal," says Morley. "It's not natural language."

Paracell came first; then the PIM was developed to run it. "In this machine, the hardware actually implements the language," says Flavors' president, David Rome. "There is no layer of software between what you want the computer to do and how the computer does it. The rules that you write in Paracell map directly into the hardware. In other words, it is real hardware that understands if-then-else rules. Our machine is designed to solve just those if-then-else, real-world

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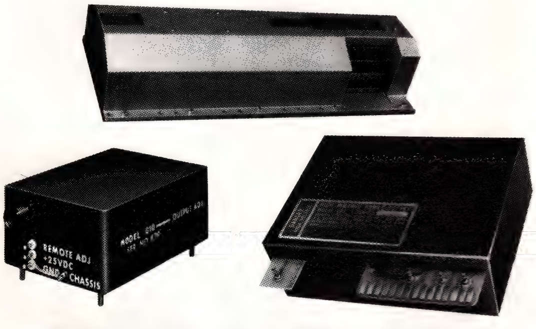

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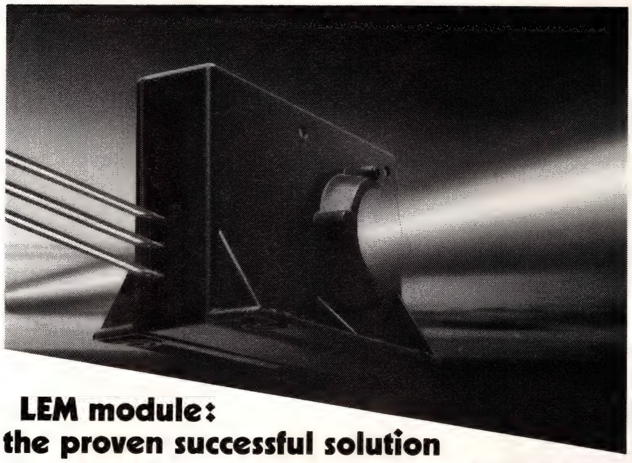

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Circle 402

problems that a human would do."

For all its sophistication, the PIM still faces a significant hurdle: market acceptance of what Rome says is a machine that "doesn't look, smell, or feel like a traditional computer—either in the way it operates on the hardware level or in the way you program it. You couldn't do general data-base or traditional mathematics-based problems on this machine. It's very specialized—it is the high end of the real-time market," he says.

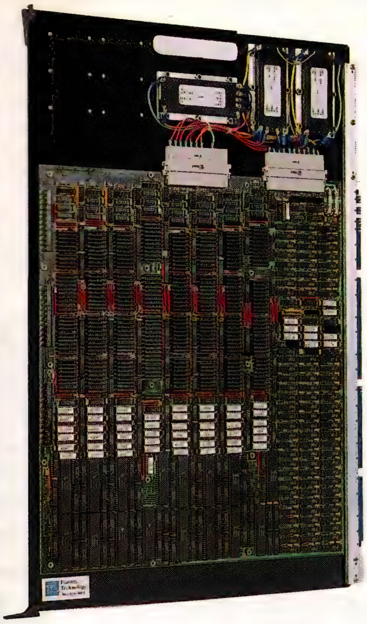
The PIM's idiosyncrasies arise from what Rome calls "several of Dick's clever techniques." For example, the PIM is a systolic, not a synchronous, computer. Where a synchronous computer queues up work and goes to the next task as it finishes the preceding one, a systolic machine runs on a fixed clock, moving to a new task every *n* milliseconds.

"That's programmed in advance," says Rome. "The reason you want systolic operation is, one, it's absolutely predictable. Two, for the right class of applications it will deliver much higher performance, because there never is any contention. There may be some wasted cycles, but the advantage of being systolic is its guaranteed predictability."

To complement its systolic setup, the PIM has what may be best described as a two-way memory bus—it runs in one direction half the time and in the other direction the other half; access is allocated in advance. Thus, the machine's 16,384 cells never bump into one other on the bus. "Every one of those cells knows exactly to the nanosecond when it can get on the bus and exactly to the nanosecond when it can write or read on the bus," says Rome.

In terms of hardware, the PIM consists of four board types: a 68030-based multiprocessor, global memory, input/output, and the controller, or "boss."

A configuration can include up to 32 multiprocessor boards, each with four 68030 user processors, a floating-point coprocessor, and one 68030 with high-speed memory that acts as a bus master. Each user processor, which has 4 Mbytes of memory for storing its rules and cache data, in turn simulates 128 software processors, for a maximum of 16,384 cells operating independently. Total memory is 1 Gbyte.



The PIM computer's global memory board contains 32 Mbytes of memory.

All other system requirements are handled by the other three boards. The global-memory board contains 32 Mbytes of 40-ns, eight-way-interleaved data memory accessible to all cells; the I/O board is a dual-ported global memory card with a data rate of 400 Mbits/s; and the boss board takes care of bus timing and includes both a serial and a shared memory.

Programming is done using the Navigator, which helps the programmer cope with the 16,384 cells by means of what Morley says is a three-dimensional spreadsheet. This is a screen of cells, three by three, behind which is another three-by-three array. The programmer works at an Apple Macintosh II.

So far, very few people outside Flavors have had a chance to program the system; Flavors will send its first PIMs into beta test after the system is formally an-

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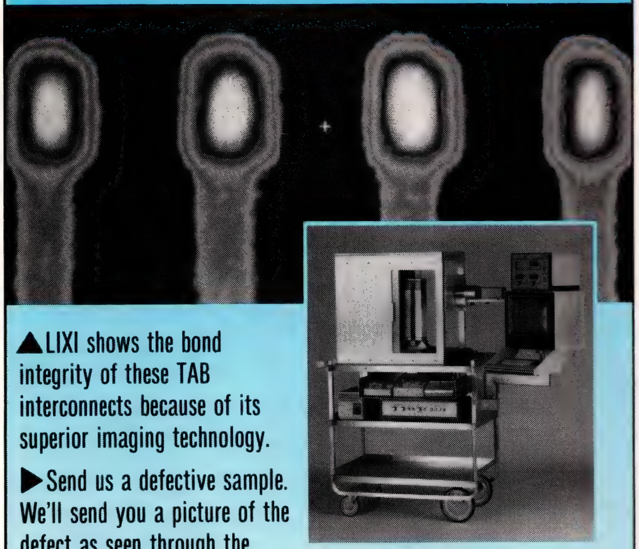

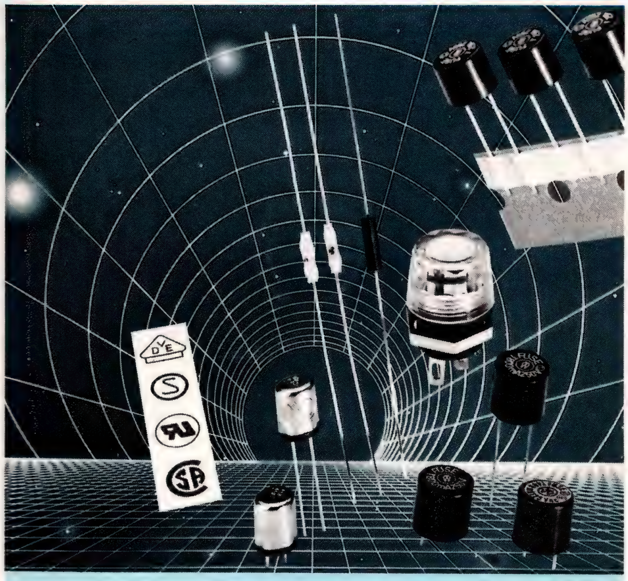

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nounced this month. But it already has won the confidence of the people who have seen it in operation.

"I took some of my experts to what Dick calls his farm—and these are very smart guys who understood immediately, precisely what Flavors is trying to do. Their reaction was very good," says Gordon Palmer, who is based in Florence, Ky., as senior vice president of Litton Industries Inc. and group executive of industrial automation. "I think it's going to become very useful to us in certain applications"—where a PIM could replace large arrays of electromechanical and programmable logic controllers.

Another observer notes the machine's adaptability to neural networks. This is "very important, because you can set up instruction sets possibly much more efficiently," says James Stark Draper, president of Ktaadn Inc., a Newton, Mass., medical-instrumentation firm. Draper worked with PIM adviser groups at Flavors.

If enthusiasm translates into sales, the PIM may signal the next new direction in computing. But without a certain degree of commercial success, it will become just another novel box. "I don't think he's sold a lot, has he?" asks Palmer. "I suppose that's the crux of any reservations I might have. I think the promise is there and it's probably a very good machine."

"My concern with things like this is that market acceptance is tough," says George Gardner, vice president of information systems at Arthur D. Little Inc. in Cambridge, Mass. "They were having trouble getting people to understand very simple AI concepts. Symbolics' machine fell on its nose in part because they had trouble getting customers to understand what it was and what logical inferences were, how you did things like that—even though it was basically an old technology."

If Gardner sounds as if he's seen all this before, he has. "We have a vast proliferation of what I consider untraditional architectures. I made a taxonomy at one point—there are several dozen different approaches. I could put [the PIM] right in that taxonomy. There are something like 78 guys out there peddling computers that are very different from what we have today." The PIM, he says, "is just another one—except this one is a little bold." *–Susan Levi Wallach*

INDUSTRIAL

THIS CAMERA BOASTS RECORD RESOLUTION

MUNICH

Advances in electronics often stem from simple tricks. Using just such a clever twist, a researcher at the Technical University of Munich has come up with a charge-coupled-device color camera that sets a record in picture resolution.

Instead of increasing the number of light detectors on the CCD sensor chip, the camera steps up the resolution mechanically by moving the chip in the image plane horizontally and vertically in tiny increments. This puts the detectors in constantly new positions relative to the object. Intermediate images are taken, which are interleaved to raise the resolution. The camera, designed for industrial uses, offers a maximum resolution of 2,994 by 2,320 pixels in an 8.5-by-6.4-mm image field. That comes to about 7 million pixels per color channel, or nearly 21 million pixels for the camera's red, green, and blue channels.

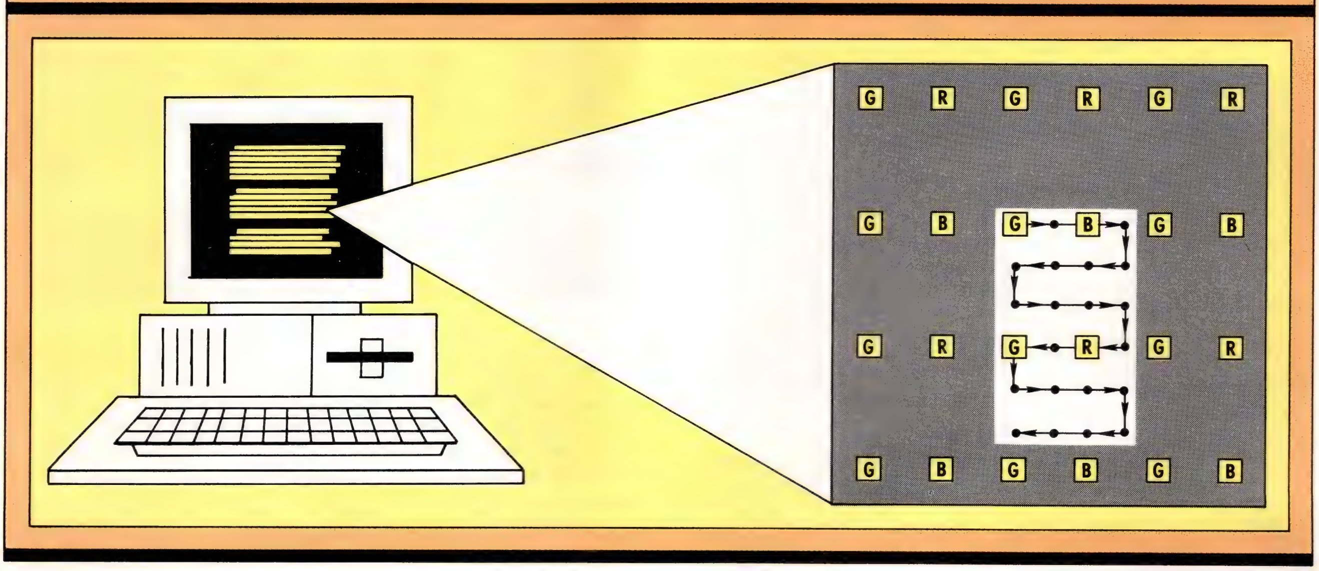
This resolution is an absolute record for a two-dimensional array sensor, says the camera's inventor, Reimar Lenz, a professor at the university's Institute for Communications Technology. The 21 million pixels, more than four times as many as for high-definition TV, provide a resolution equivalent to that of a 35-mm color negative or slide.

Unlike most developments in German electronics, the idea became a product in short order—about a year. Since the summer of last year, when he got the idea, Lenz worked on his own to develop an experimental camera and enlisted Kontron GmbH in Eching to produce and market the equipment.

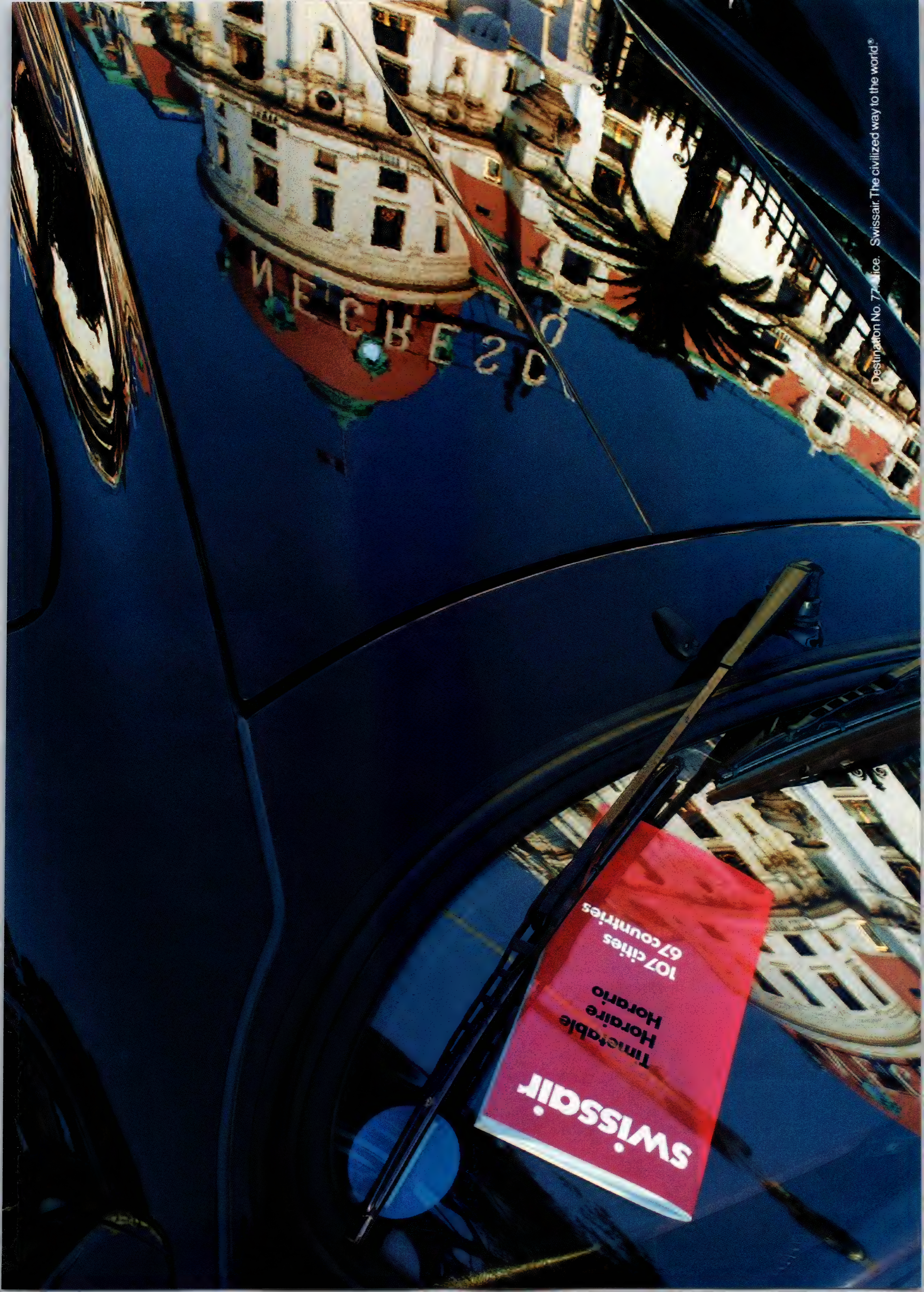
The conventional way to increase a CCD sensor's resolution is to increase the chip's integration. But that's getting more and more expensive as the limits of semiconductor technology are approached. Today's top resolution stands at 2,048 by 2,048 pixels for an 18.4-by-18.4-mm noncolor sensor that Eastman Kodak Co. showed last spring at the Hanover Fair in West Germany for $75,000.

By contrast, Lenz's sensor-displacement technique makes for relatively inexpensive equipment. The whole Kontron camera, including the sensor, electronics evaluating circuitry, and a built-in analog-to-digital converter, sells for just $25,000. What's more, the camera is flexi-

BOOSTING RESOLUTION



The CCD sensor is mechanically displaced in two directions in the microscanning technique. Intermediate pixels are generated between original pixels. Developed at the Technical University of Munich, it has a basic resolution of nearly 300,000 pixels.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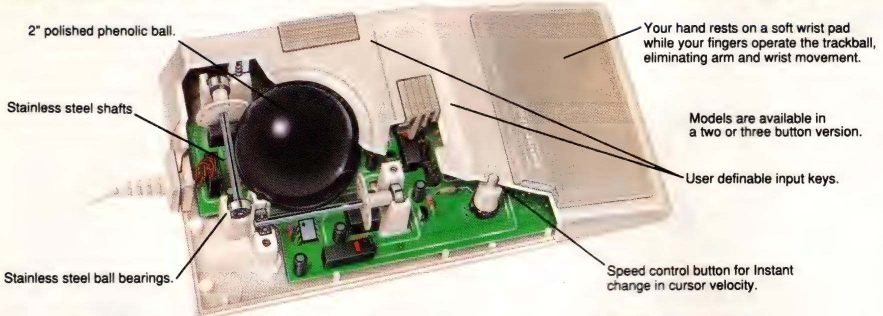
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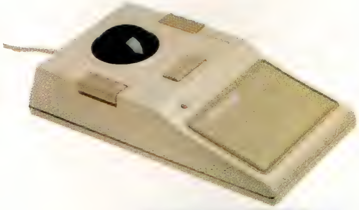

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Circle 472

ble in that its resolution, and hence the signal read-out speeds can be programmed. This has given the camera its name: ProgRes 3000, for programmable resolution 3,000 (pixels in a line).

The camera's CCD sensor chip has a basic resolution of 499 by 580, or nearly 300,000 pixels. Unlike other devices, the sensor is laid out so that the light-sensitive areas, the detector apertures, take up relatively little space.

After the first image is taken, the sensor moves two-dimensionally in incremental steps, each step amounting to a fraction of the spacing between detectors. As a result, at each step, the sensor produces a new image. These intermediate images are interleaved to bring up the resolution.

Affecting the sensor movements are small piezo positioning elements attached to the sensor. Voltages applied to these elements cause them to expand and contract, which in turn displaces the sensor in a procedure called piezo-controlled aperture displacement. The sensor can move over a maximum distance of 50 μm. The displacement accuracy is ±200 nm, and the displacement speed is one second for 12 different sensor positions.

LIMIT REACHED. In principle, Lenz says, the number of intermediate images, and thus the obtainable resolution, can be raised further. However, a practical limit is reached when the pixels start to overlap by more than 50%. In that case they would no longer yield any useful information.

The images are read out individually in 40 ms, digitized at a 10-MHz scan rate and at 8-bit resolution per color channel, and finally stored in a host computer that can be attached to the camera. Because of the large amount of data involved, this process takes time: 8 seconds for 28 Mbytes of data at maximum resolution. Given this long processing time, the camera is unsuitable for taking moving pictures.

So its applications are in still photography, particularly for taking the high-quality pictures needed for color ads or documentation. Coming in handy here is the sensor's programmable resolution. It can be set from 499 by 580 pixels in steps up to the maximum of 2,994 by 2,320. A reproduction with a color laser printer on letter-sized paper yields 10 pixels per mm, which compares with the figure for high-quality prints.

Since the images can be stored as digital signals, large electronic tape-based archives can be built up in which access times to the digitized pictures are much shorter than they are for pictures that are stored in their physical form.

That's beneficial in archiving the images of pieces of art, as well as in medical applications. Because of the 2-d array sensor's inherently high geometrical accuracy, applications in photogrammetry and quality control in machine vision are also possible. *–John Gosch*

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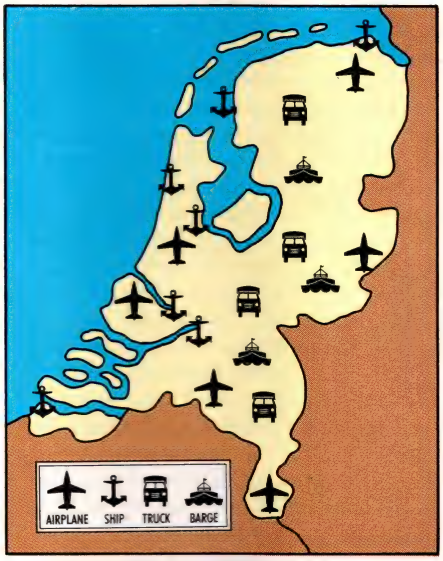

SOME FACTS ABOUT HOLLAND

- ☐ Working population: 6.5 million
- ☐ Population within a 300-mile radius of Amsterdam: 165 million
- ☐ 1988 Exports: 8.7 billion Dfl (US$4.35 b)
- ☐ 1988 Imports: 15.0 billion Dfl (US$7.5 b)
- ☐ Port of Rotterdam: 273 million tons cargo handled in 1988, up almost 7% from 1987
- ☐ Share of cross-border road transport within the EC accounted for by Dutch haulers: 40%
- ☐ About 1,500 U.S. firms invested in Holland
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Circle 240

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DALLAS

Down time: it's the dirty little secret of local-area networking, except that the cost of a large network laboring under partial disabilities 6% of the time is not little. Partial disabilities—events that degrade performance but do not necessarily render the network totally inoperative—cost larger companies $3.5 million a year in lost worker productivity and $600,000 a year in lost revenue, according to a study by Infonetics Inc., a Santa Clara, Calif., market research firm.

The $3.5 million productivity loss is "actually a conservative figure," says Infonetics vice president Steve Spanier, "because we took into account those instances when people could be productive in other activities even though they could not use the network."

Infonetics released the results of its telephone survey of 100 Fortune 500 companies at last month's NetWorld '89 show in Dallas. The networks covered in the survey were large—averaging 320 nodes—and more important to their companies all the time. "There's a movement toward taking mission-critical projects off minicomputers and mainframes and moving them to the network," says Spanier. The average number of disabilities was 24 per year for an average period of 4.8 hours. When a network develops problems, a company's typical response is to upgrade the network. Companies in the survey spend, on average, $670,000 a year doing just that.

"A lot of the money for performance upgrades was not wisely spent, because it does not solve the problem of disabilities," says Harry Saal, president of Network General Corp., the San Jose, Calif., instrument manufacturer that paid for the study.

Saal cites the study as proof that the time for network analyzers—such as Network General's Sniffer—has arrived. Although the number of network disabilities tended to rise with the number of nodes, protocol analyzers were effective in controlling malfunctions. Even though the average number of nodes in networks monitored by protocol analyzers was twice that of nonmonitored nets, the number of disabilities was virtually the same, says Saal.

As LANs become of more strategic importance to big companies, demand will increase for network or protocol analyzers that keep them operating at high efficiency. Among the companies marketing analyzers are Excelan, Hewlett-Packard, M-Test Equipment, and Spyder Systems.

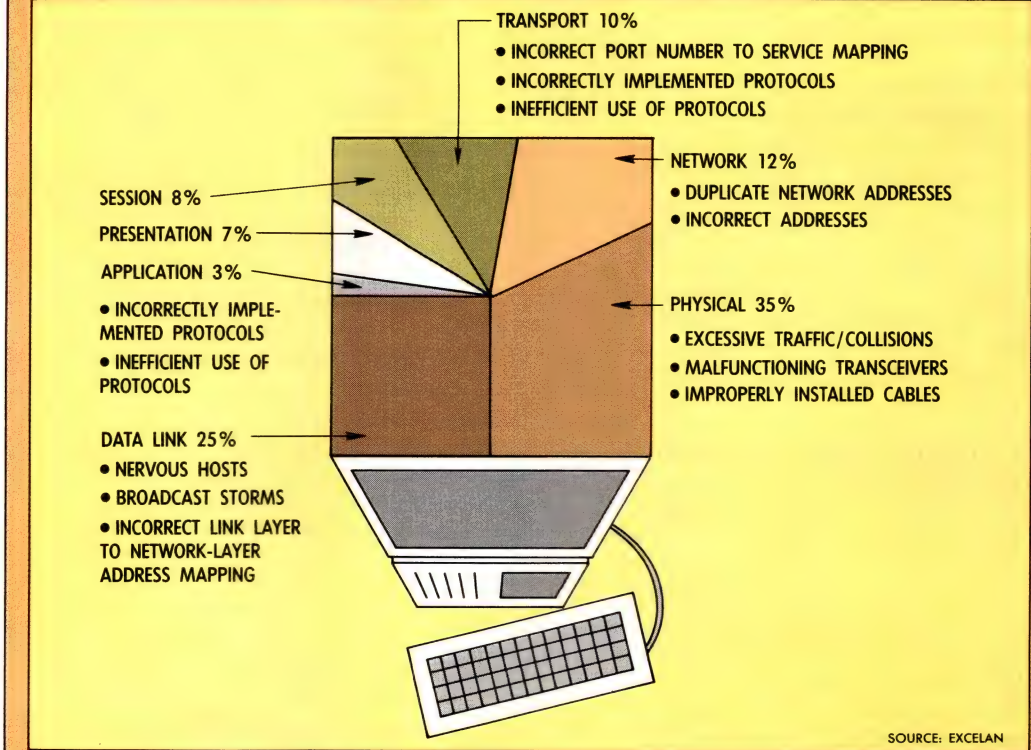
LOW WOES. Excelan has studied the problem of network disabilities from another perspective—where they occur in the seven-layer stack of the Open System Interconnect protocol. "We found that the bulk of the problems occur at the lower layers—faulty wires and kinked cables," says John DeVries, marketing manager for Excelan's LANalyzer. "But network managers have no visibility there—not the way they do in the higher levels such as the application level, where they can call the program onto the screen."

In large nets, managers cannot easily survey the physical connection, so many network-monitor instruments include time-domain reflectometers. "Once you've verified that the physical stuff is intact, you have to monitor proactively," says DeVries. Although physical connections may be solid, other problems can sap available bandwidth. Examples are broadcast storms or nervous hosts—computers that keep broadcasting their addresses.

"There is still a good deal of fear and loathing when we start to talk about protocol analyzers," says Christoper Ray, president of San Francisco-based M-Test. Instruments developed by the LAN community still can't capture all the data on the network so that each node can be examined at the same trigger point. "The real problem is knowing where to look, and the only way to do that is to take an overview of the network," he says.

To its protocol expertise, acquired from years of working in wide-area networking, M-Test adds very high-speed hardware to solve the problem. Its product—the Comtest Network Analyzer—is the next generation in LAN troubleshooting instruments. Introduced at NetWorld, Comtest can analyze 100% of an Ethernet data stream. It includes sophisticated statistical-analysis software and automated TDR procedures to calculate overall performance statistics—not just the performance of four-node pairs, as does the competition. *–Jack Shandle*

WHAT CAUSES NETWORK PROBLEMS?



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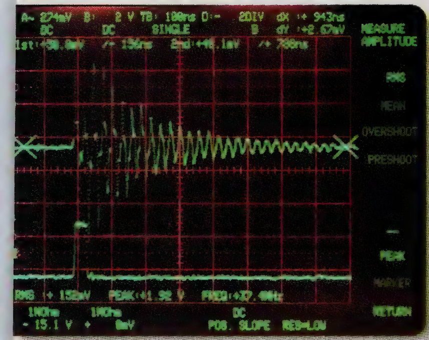

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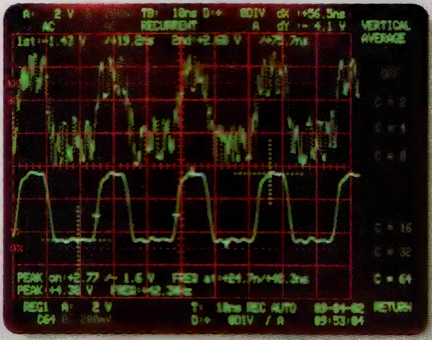
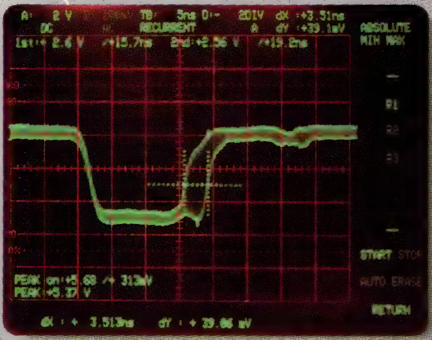
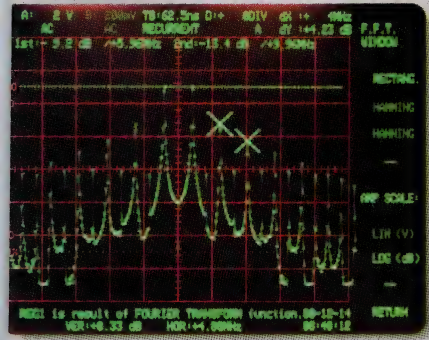


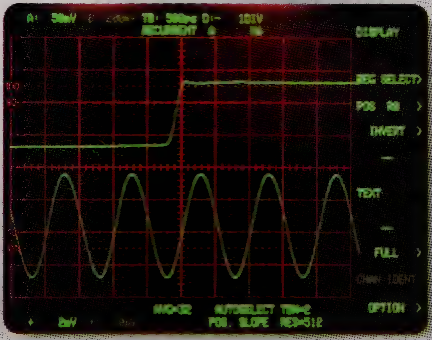
The averaging mode eliminates noise and optimizes signal information content



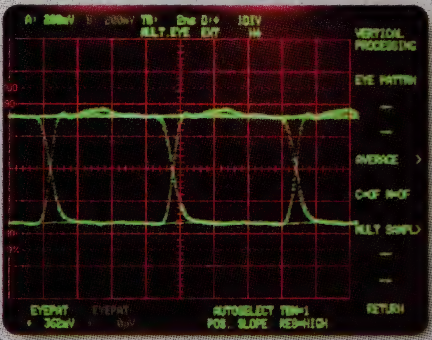
The envelope mode makes it easy to log signal variations in amplitude and time



Optional FFT functions allow quick display of power spectra in the frequency domain



PM 3340's ultra-fast 175 ps risetime allows secure digitization of even the fastest signals



An 'eye pattern' display (PM 3340), used for assessment of PCM communications signals

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HERE COME AFFORDABLE EQUIPMENT AND ICs

LONDON

The prices of millimeter- and microwave-link equipment, as well as the gallium arsenide semiconductors needed to make it, should come tumbling down now that the British government has made a move that seems calculated to stimulate demand.

The recent action by the Department of Trade and Industry to confirm its decision to allocate frequencies in the 40-GHz band for microwave TV distribution systems might do the trick.

The move has not calmed equipment makers and potential users. Given an opportunity to argue the case against the use of such high frequencies, some 30 vendors had pointed to the shortage of affordable equipment and components that could operate at that level.

RULED OUT. Earlier, the department had disappointed many of these manufacturers by ruling out original plans for the systems to operate at either 2.5 GHz or in the 27-to-29-GHz bands. An alternative proposed by some industry commentators was to pitch the services in the 12-GHz band. However, that part of the spectrum is allotted to satellite TV broadcasts and to the outside broadcast links used by the British Broadcasting Co., the Independent Broadcasting Authority, and British Telecom.

There is still a faint glimmer of hope that 12 GHz may be used. Government officials say they will review the need to make frequencies in the 12-GHz region available to microwave video distribution systems "in a year or so." By that time it expects that "a number of uncertainties should have been resolved."

While the new proposal fits neatly with international agreements on the use of the 40-GHz bands for broadcasting, manufacturers will be faced with a dire shortage of low-cost circuitry capable of working at that frequency.

The major use intended for lower-power microwave communications links is as an alternative to coaxial or fiber cable for the distribution of TV signals to homes in communities considered too small or too widely spread to justify the cost of burying cable. They may also be licensed for the distribution of video signals—such as those from surveillance cameras, videoconferencing systems, or high-speed telemetry data—around large, self-contained complexes: airfields, college campuses, petrochemical plants, and the like.

Among those with prototype equipment operating in field trials is British Telecom, whose Millimetre-wave Multichannel Multipoint Video Distribution Service operates at 29 GHz. Last October, BT started testing a system in Sachsmundon in Suffolk.

At that time the company had already started a development program to build low-cost GaAs integrated circuits for use at 29 GHz and had designed an inexpensive domestic antenna.

The question now is whether 40-GHz circuits could be developed to retail at consumer electronics prices by 1991, which is when the government wants to issue franchises to service operators.

A British decision to use 40-GHz band for microwave TV systems is key

Reasons for the choice include pressure on the 2.5-GHz band coupled with "uncertainties surrounding possible international developments and the limited amount of spectrum that could be best made available." The higher band at 27 to 29 GHz was ruled out since "the 40-GHz band has similar characteristics and the significant advantages of larger amounts of spectrum, no existing incumbents, and the fact that it is in part already designated internationally for broadcasting applications," says Nicholas Riddley, secretary of state for trade and industry.

The government says that at 40 GHz, 20 or 30 channels could be allocated to BT's microwave TV distribution services, which some have argued would be necessary if the technology is to play a long-term role in the local-delivery franchises of the future. However, at this frequency, the service range would be restricted to around 2.5 miles, and the cost of equipment might be high.

That is why the government has not ruled out the use of 12 GHz, which, it acknowledges, would increase coverage to 10 to 12 miles in diameter. But it says that only six channels could be made available at the lower frequency, and there may be conflict with the need for more direct satellite broadcasting channels, which have priority in the band.

Microwave industry insiders suspect that in reality the government wants to assure the continuing availability of GaAs millimeter and microwave ICs, which the UK semiconductor industry has found too expensive to develop without a guaranteed market. They point to an earlier decision that operators of personal communications networks would be able to use microwave radio links in the fixed infrastructure of their networks. And the government has stipulated that these links would have to "operate at millimeter wavelengths"—that is, at frequencies above 30 GHz. *–Peter Fletcher*

CONSUMER

TURNING THE PHONE INTO A 'LOW-END WORK STATION'

EINDHOVEN, THE NETHERLANDS

If prognostications from Philips International NV are correct, the home telephone will undergo drastic changes in the coming decade. Today's simple dial- or button-operated phones will be replaced by features-laden terminals complete with keyboards and displays to accommodate not only voice but also video and graphics functions.

The 1990s will see the home phone turn into "nothing less than a low-end work station," predicts Peter Draheim, director of the business unit for integrated circuits at Philips' Components Division in Eindhoven. Philips, Europe's No. 1 chip maker, is gearing up to build and sell components for the phone of the future. The company is launching another round of advanced parts for terminal equipment—this after introducing late last year a series of devices compatible with the integrated services digital network [*Electronics*, January 1989, p. 32H].

Philips believes the new devices—among them a microcontroller, an echo canceler, and dialers—will solidify its position as Europe's top producer of ICs for telephone sets. Last year, the company's overall telecom chip business came to around $100 million. Draheim expects that total to at least double by 1993, with sales growth for phone-terminal devices outpacing that for general telecom applications. He foresees particularly strong growth in the U. S., with the Philips affiliate Signetics Corp. of Sunnyvale, Calif., carrying the ball.

STRONG AREA. That the Dutch company is focusing on phone terminals is no accident. Traditionally, the consumer-products market has been a strength for Philips. It's no surprise, then, that the company's components activities have gravitated toward parts for consumer products at the expense of devices for, say, telephone exchanges and the like.

Thus, in line with past practices, "we are aiming our new devices again at a consumer application—at the work station in the home, a product in which consumer circuits meet up with data-processing and communications technology," Draheim says. The new ICs are the forerunners of what's coming for low-end home work stations, he adds.

For its consumer circuits, particularly those for portable equipment, Philips has emphasized low power consumption. The company now builds most of its new phone circuits using a power-cutting technology it calls Sacmos, for self-aligned CMOS. Philips developed Sacmos a few years ago at its labs in Zurich, Switzerland, for use in making semiconductors for watches and clocks.

For the new microcontroller, the Sacmos process uses 2.0-μm design rules, but it provides a packing density equivalent to that obtainable with 1.0-μm CMOS technology. In effect, Sacmos allows for smaller circuit structures, and hence transistors that are smaller than CMOS devices. The Sacmos process achieves higher packing densities because it all but eliminates the spacing between the contact openings and the isolation edge, a region that contributes nothing to CMOS gate operation and wastes die space.

WASTED SPACE. In the process, a thin—only 60-nm—silicon-nitride isolation layer is placed above the gate region. This layer replaces the wasted spacing used in CMOS devices to isolate the gate from the source and drain regions.

Because Sacmos transistors are smaller than CMOS versions, the connections between them are shorter and the diffusion areas smaller. This helps reduce parasitic capacitances and drain resistances, improving circuit speeds. Further, production equipment for 2.0-μm chips is widely available and costs less than that for 1.0-μm devices. The upshot is that 2.0-μm Sacmos circuits are less expensive to make than 1.0-μm CMOS parts of the same packing density.

Of the new Philips chips, the microcontroller clearly stands out. The PCF86C410, an 80C51-based device, works from power supplies as low as 1.5 V—the lowest for any such component on the market, Philips says.

The low power needs "will open a broad new market for single-cell applications in telephony and related areas," says Ton van Kampen, a product marketing manager in the Components Division. He points to pocket telephones and other portable terminal equipment, such as cordless and cellular phones, as possibilities. The 86C410 also targets feature phones, telefax machines, and answering devices. Although designed primarily for communication terminal equipment, the controller can be used in computer peripherals, smart cards, instrumentation, and industrial controls as well.

Philips' new family
of terminal chips
aims to tap that market

Two new operating modes also help the 86C410 cut power consumption. Normally, the 16-MHz microcontroller draws 1 mA from a 3-V power supply at a clock rate of 3.58 MHz. In idle and power-down modes, current consumption is cut to 0.5 mA and 1 μA, respectively.

The 86C410 can operate at low clock frequencies. The chip's oscillator circuits work down to 32 KHz; with external oscillators, the controller operates even down to dc levels, which means the clock can be turned off. When the clock is turned back on, the 86C410 resumes the operation it was performing. The result is even lower current drain, because the controller lies dormant until the clock stream resumes.

Low power consumption is also typical for Philips's other new entries. Among them are two dual-tone multifrequency dialers, the PCD4420 and PCD4421. These devices can redial up to 23 digits and meet international distortion specifications without the need for external components. They operate from power supplies of 2.5 to 6 V and consume just 1.5 μA in standby mode. During a conversation, they draw a maximum of 150 μA, and during dialing, 1 μA. The Philips devices are pin-compatible with Gould AMI Semiconductors' S2569A and SGS-Thomson Microelectronics' M6569 DTMF dialers, and they have special private-branch-exchange features, such as pause, flash, access, and disconnect.

CONNECTIONS. The new PCB2325 extended data-rate adapter, also a Sacmos device, interfaces V- or X-series terminals to 64-Kbit/s channels in accordance with ISDN standards. It also connects terminals to other 64-Kbit/s networks, such as Philips' integrated-services-terminal bus, an ISDN-compatible voice and data local-area network.

Among the 2325's special features are network-independent clocking, which allows the chip to connect to modems running on their own clocks, and submultiplexing, which permits eight extended data-rate adapters to share one 64-Kbit/s channel. The device also supports a multiple sampling method with transition coding. This converts data from asynchronous terminals at any speed up to 19.2 to 64 Kbits/s.

The 2325, also a Sacmos device, typically draws less than 8 mA from a 5-V supply. In power-down mode, consumption is less than 0.2 mW.

Van Kampen says the PCB2391 is the first single-chip ISDN echo canceler to have on-chip layer 2 functions relating to the ISDN control channel. Optimized for PBX extension lines up to 2 km, the device supports remote multiplexers and can operate in public exchange lines serving nearby subscribers. Also a Sacmos part, the 2391 consumes less than 100 mW in operation and less than 40 mW in the power-down mode.

Then there is the Signetics-designed NE8392A coaxial transceiver interface chip for LANs. Using advanced bipolar technology, the device links data terminal equipment to an Ethernet or Thin Ethernet coaxial network cable.

It provides for key network functions—receiver, transmitter, collision-detection, and oversized-data-packet handling. *–John Gosch*

MEDICAL

PHILIPS GETS BETTER QUALITY IN X RAYS

AACHEN, WEST GERMANY

Researchers at Philips Laboratories in Aachen have achieved an impressive breakthrough in the processing of X-ray images by devising a way to use digital techniques that greatly improve signal-to-noise ratios.

The key to the process is amorphous selenium. After five years of development, Philips has succeeded in producing photoconductive layers of amorphous selenium as an image-storage medium for digital radiography. Researchers Ulrich Schiebel and Walter Hillen have built an experimental X-ray exposure system that yields large-format digitized images of a much higher quality than those captured on standard X-ray photographic film.

The images feature an S/N ratio that is limited only by the absorbed X-ray quanta over a wide dose and spatial frequency range; the selenium's intrinsic noise is negligible. Not only does the process yield high image quality, but it also minimizes patients' exposure to X rays, Schiebel says.

The system boasts a wide exposure range—from 0.2 to 200 microgray. That suits it for virtually all important medical applications—imaging body parts such as the skull, chest, and extremities—in which film is used today.

Although researchers at other facilities are also investigating ways to obtain higher-quality images and are experimenting with improved-performance equipment, the image quality the Philips system achieves has not yet been matched, according to Schiebel.

In Philips's experimental system, a

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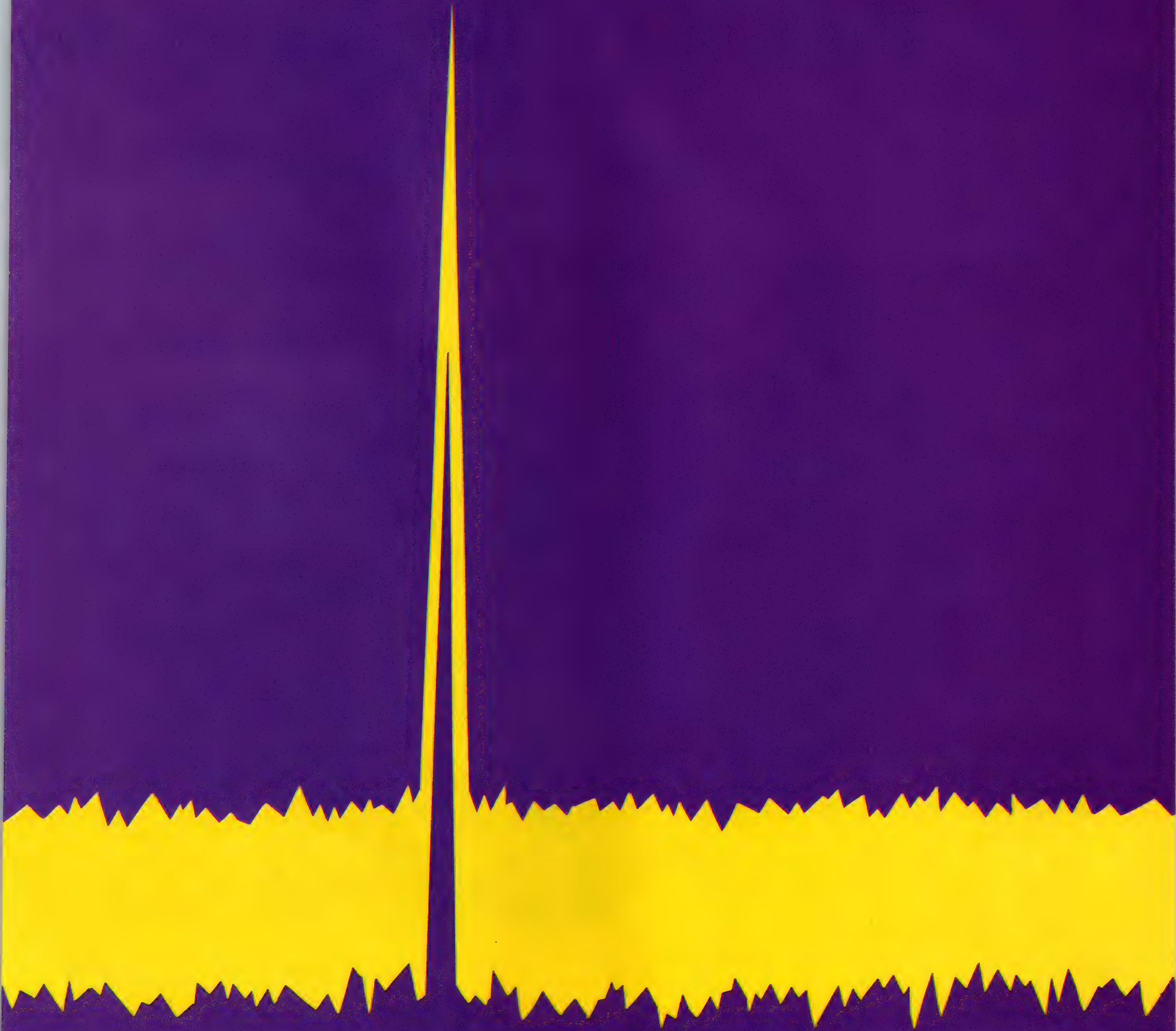

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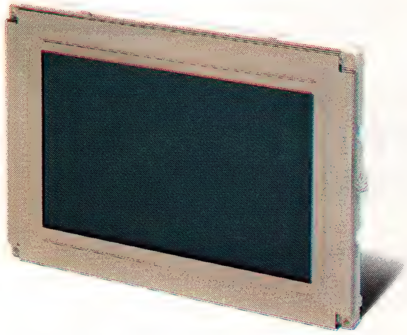

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Circle 278

flat, fan-shaped X-ray beam is projected through a slit aperture near the X-ray source. The beam traverses the part of the body to be imaged.

After passing through another slit aperture, the beam then impinges on a rotating aluminum cylinder covered with a layer of amorphous selenium. The selenium's negligible intrinsic noise is one reason for the high image quality; the two slit apertures are also major factors. They suppress scattered radiation that would otherwise cause image blurring and loss of contrast.

ELECTRON HOLES. Before the exposure, the selenium layer is given a homogeneous positive surface charge. When the X-ray beam hits the selenium, the element is discharged at the contact point. The process creates pairs of electron holes that travel to the aluminum substrate while the electrons move to the layer surface to recombine with the positive surface charge.

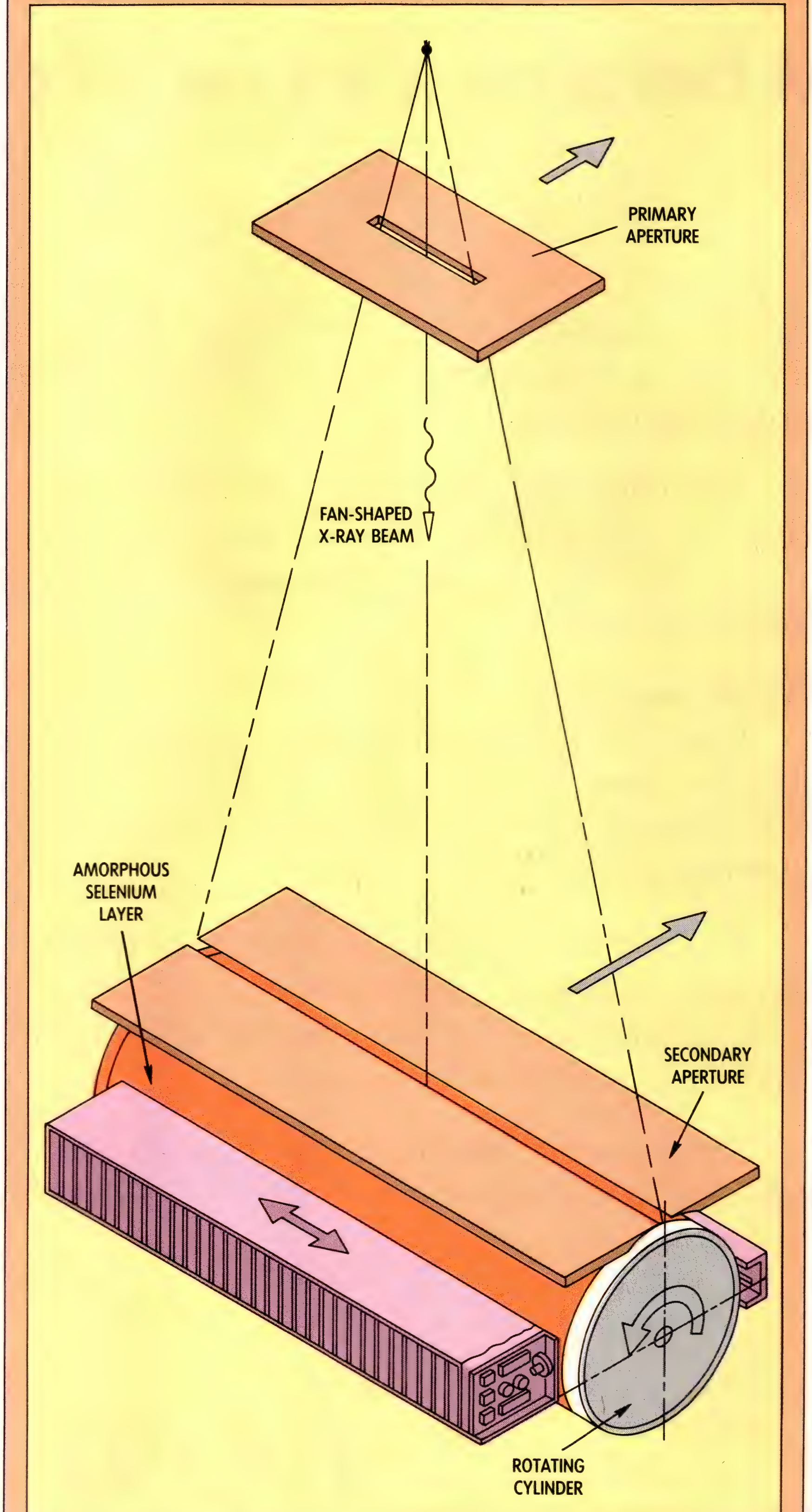
As in xerography, a latent charge image is stored on the selenium's surface after the exposure. Its charge density is proportional to the intensity of the incident X-ray beam.

The X-ray source and the selenium-covered cylinder move together so that the part of the body to be examined is completely scanned.

The image, recorded as a charge distribution in the selenium, is read out with high-resolution electrometer probes arranged in a linear array.

The probes' output signals are amplified, digitized, and stored for further processing. *–John Gosch*

HOW PHILIPS GETS BETTER X RAYS



In the Philips scheme, a flat X-ray beam travels through two slit apertures to a cylinder coated with selenium, which boasts low intrinsic noise. The slit apertures suppress scattered radiation that would otherwise cause image blurring and loss of contrast.

SOLID STATE

PLESSEY'S 10,000-SWITCH CHIP IS READY TO ENLIST

ROBOROUGH, ENGLAND

Plessey Semiconductor Ltd. is producing its largest chip ever: 20 mm measured diagonally. Built using a standard CMOS process at Plessey's Roborough wafer fab, it comprises an array of 10,000 simple switches together with on-chip signal processing and memory circuits and is headed for a classified military system.

The chip provides a matrix of 10,000 connecting pads, one for each switch element. These connect by solder bumps to the back of a similar-sized monolithic array of 10,000 pyroelectric thermal sensors defined in a slice of rare-earth crystal. Along with its silicon slice, it forms a high-resolution thermal imaging head being built under a Minsitry of Defence contract. Output is in the form of a serial video signal. *–Peter Fletcher*

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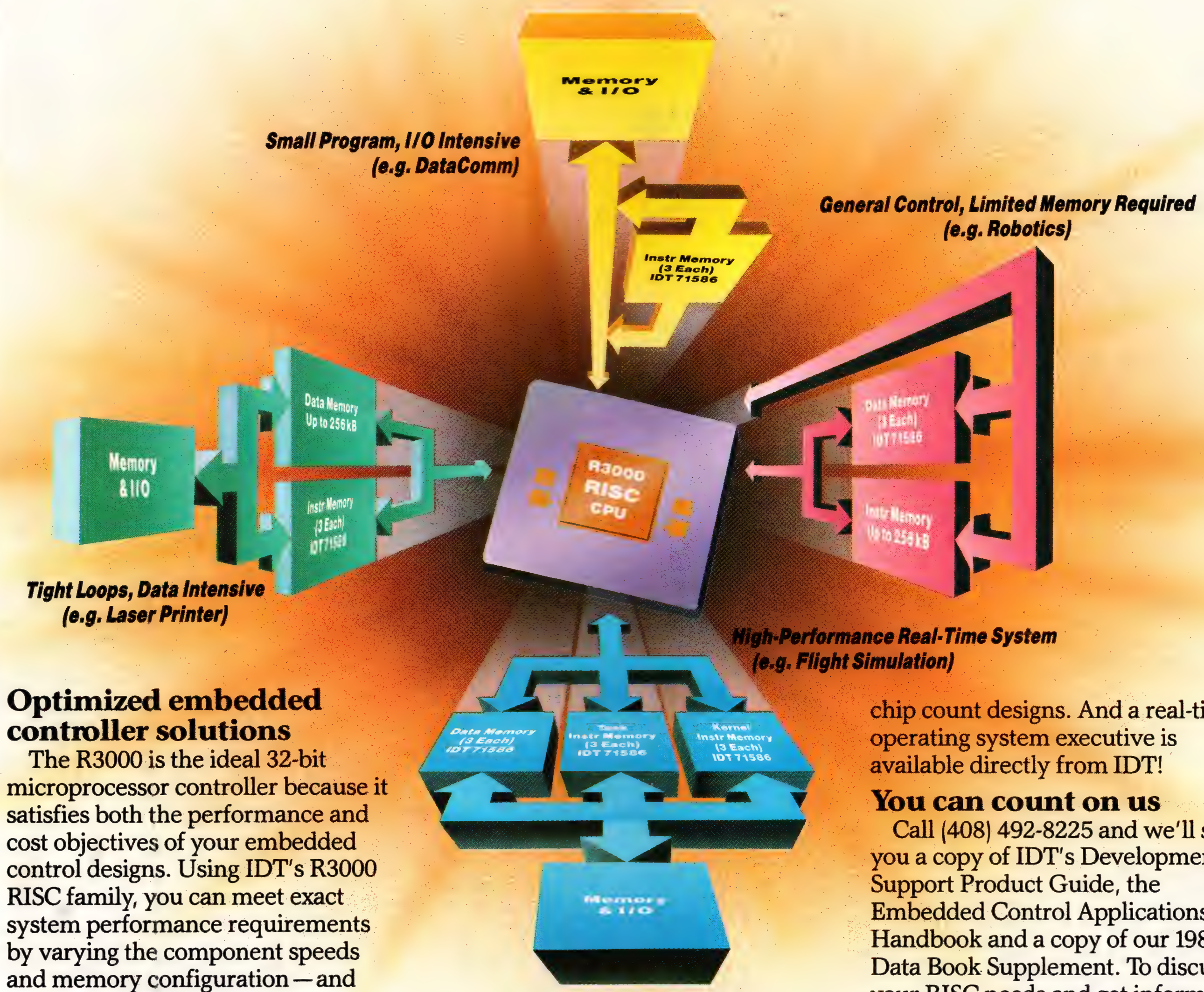
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Circle 216

OCTOBER 1989

EUROPEAN OBSERVER

INMOS SLASHES PRICES ON THE TRANSPUTER . . .

Inmos Ltd. is mounting an aggressive campaign to get its Transputer designed into more systems. The Bristol, UK, company, now part of SGS-Thomson Microelectronics, has announced a low-cost version of the 32-bit parallel-processing chip, price cuts of 40% to 70% on available versions, and a raft of software support packages to make programming it easier. The new "thrift-line" Transputer, the T400, is a 32-bit integer processor for embedded applications; it crunches 10 million instructions/s. The cost-cutting packaging tricks that let Inmos sell it inexpensively—just $20 in quantities of around 50,000—also helped the company slash prices on other Transputers, says managing director Mike White. For example, the T800-20, once priced at $300 apiece in 1,000-unit lots, now sells for $195. Meanwhile, to make programming the Transputer simpler, Inmos has packaged some 17 software tools, including development systems and compilers, that offer an interface to high-level languages such as C, Fortran, and Pascal. ☐

. . . AND ANNOUNCES A NEXT-GENERATION VERSION

Hold on to your hats: the next Transputer will sustain 100-mips, 20-megaflops performance, says Pasquale Pistorio, president and CEO of SGS-Thomson Microelectronics. The company's Inmos subsidiary will begin shipping samples of the next-generation 32-bit floating-point processor in early 1991. Now called the H1, the chip will be built with a new 1.0-μm double-level-metal process. It will be instruction-set-compatible with existing Transputers while offering 10 times the computing clout. With hardware support for message multiplexing and standard operating systems, plus network message through-routing, "the H1 will make the development of multiprocessing systems extremely simple," says managing director Mike White. ☐

FERRANTI'S U. S. SUBSIDIARY UNDER INVESTIGATION

A financial imbroglio involving a U. S. subsidiary is making life grim for Britain's second-largest defense electronics contractor, Ferranti International Signal plc. At issue is $225 million in missing money and a possible case of fraud involving contracts held by ISC Technologies Ltd. of Lancaster, Pa., at the time it merged with Ferranti in 1987. Scotland Yard's Serious Fraud Office is looking into the case, as is the Pentagon's Defense Criminal Investigation Service. The contracts concerned cover a series of apparently covert arms deals in the Middle East along with a missile contract that was, says one observer, "at best dubious, at worst nonexistent." The net effect for Ferranti is to turn a financial year termed "disappointing" by chairman Sir Derek Alun-Jones into a disaster. Early in September, Ferranti had dealings in its shares suspended on the London Stock Exchange. Alun-Jones is looking to raise $150 million to reduce Ferranti's debts by selling some nonelectronics segments of the business. ☐

THE CORDLESS PAY PHONE ARRIVES IN BRITAIN

The first of Britain's "telepoint" mobile communications services is now up and running. Phonepoint—a consortium made up of British Telecom, Deutsche Telekom, France Telecom, Nynex, and STC—opened its digital-radio public service last month. Telepoint operates like a cordless pay phone. A user will purchase a pocket-size cordless telephone that can be used with public base stations, which Phonepoint plans to install at 500-meter intervals in most UK towns. The phones use digital-radio, frequency-division multiple access so each base can handle up to 40 calls simultaneously. Three other telepoint operators expect to be operating in the UK by year's end. ☐

EUROPEAN OBSERVER

EAST GERMANY INTRODUCES ITS FIRST 32-BIT PROCESSOR

East Germany has given itself a birthday present: the country's first functional 32-bit microprocessor. Representatives of the state-owned electronics combine VEB Mikroelektronik in Erfurt, where it was developed, presented the device to Erich Honecker, Socialist Party chief and head of government, on the 40th anniversary of the founding of the German Democratic Republic, as East Germany is officially called. The U80701 follows hard on the heels of a 1-Mbit dynamic random-access memory the East Germans should soon have in pilot production [*Electronics*, April 1989, p. 18]. The processor operates with a 40-MHz clock, features a throughput of 1 million instructions/s, and integrates about 130,000 transistors on an 85-mm^2 chip. The real test for East Germany, say Western observers, lies in turning out the device in volume. ☐

THERE'S A NEW WORK STATION SPIRIT AT ESPRIT

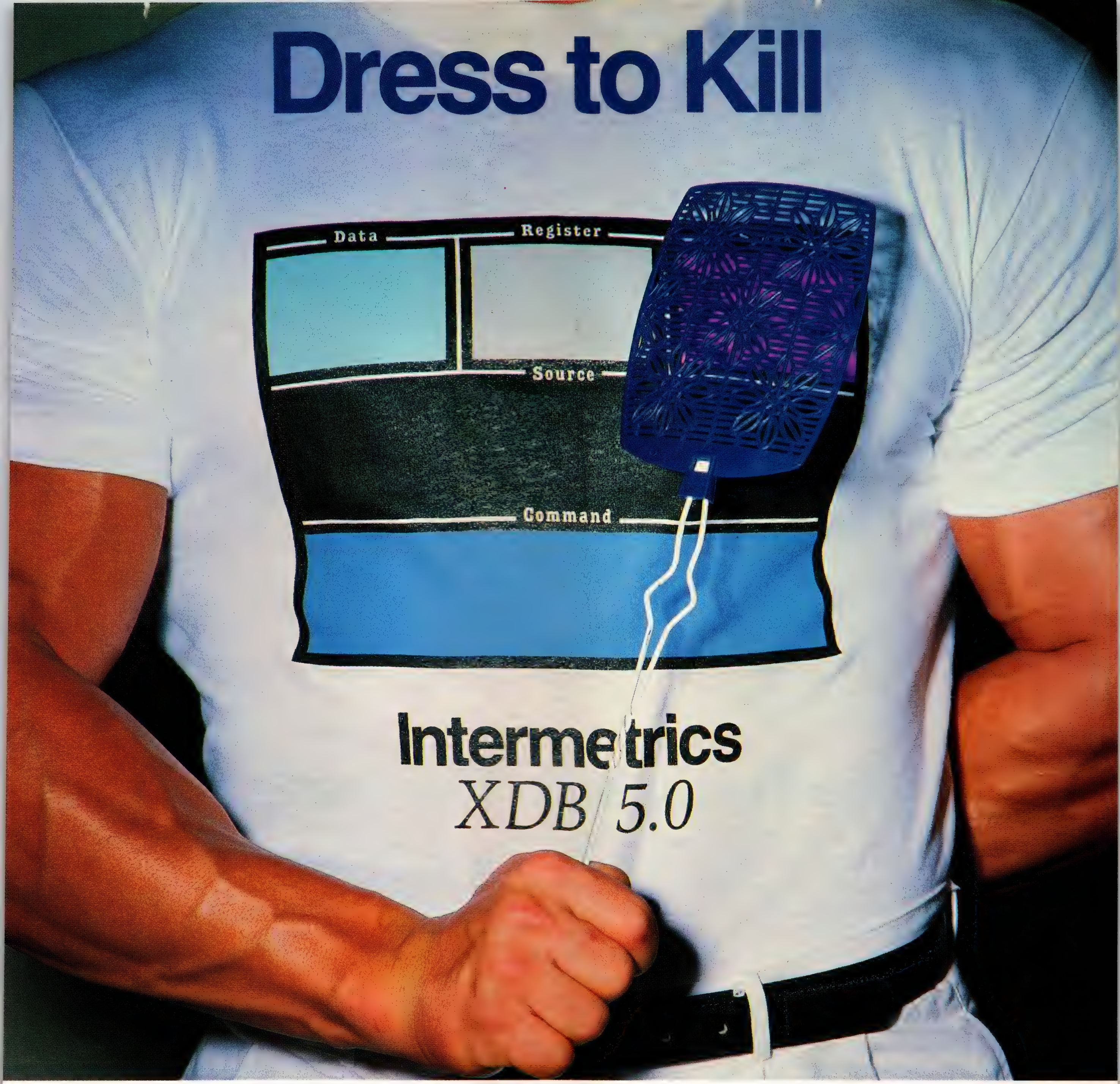
A high-performance engineering work station boasting computing power of 1,000 mips and 1,000 megaflops: that's the goal a seven-member European consortium wants to reach by the mid-1990s. Four companies and three universities are cooperating in developing the Spirit work station, a project within the European Strategic Program for Research and Development in Information Technology (Esprit). "Spirit will enable the European industry to compete successfully against non-European companies on the high-end work station market of the 1990s," says John Zabolitzki, managing director at West Germany's Kontron Electronik GmbH and head of the project. The Unix-based machine will incorporate standard processors as well as processors for artificial intelligence, plus a subsystem implementing 3-d graphics. Besides Kontron, participants are ACE Associated Computer Experts of the Netherlands, British Aerospace Systems and Equipment, and Caption of France, as well as the University of Sussex and Queen Mary College in the UK and the University of Tübingen in West Germany. ☐

DOES EUROPE NEED TO CONCENTRATE ITS DEFENSE INDUSTRY?

Philips International NV of the Netherlands is negotiating a deal to transfer its defense activities to France's Thomson-CSF. This, Philips says, is in the interest of promoting European integration and concentrating Europe's defense industry. Among the specifics being negotiated between the two electronics giants is the transfer of a majority interest Philips has in Hollandse Signaalapparaten NV, a $450 million producer of radar and fire-control systems, military communication equipment and networks, and command and control systems. Also being discussed is Thomson-CSF's acquisition of a minority interest in the defense activities of MBLE, Philips' Belgian subsidiary, and 100% interest in the defense activities of the French company TRT, in which Philips has a 49% interest. An agreement is expected by year's end. The increasing cost of developing and producing defense equipment make cooperation and larger manufacturing units necessary, Philips says. ☐

HERE'S HIGH-FLYING ENTERTAINMENT FROM PHILIPS AND WARNER BROS.

It's official: TV will take to the air in the form of Airvision. After tests with a number of airlines, Philips International NV will commercially offer the TV system, which it developed in a joint venture with Los Angeles-based Warner Bros. Inc. The Dutch company's mini-LCD color TV set can be mounted into the backrest or armrest of airline seats, where passengers can tune it to any of six TV programs. The 3-in., active-matrix LCD provides 92,160 pixels for high resolution. It has been put through its paces on Alitalia, British Airways, Northwest Airlines, and Qantas. ☐



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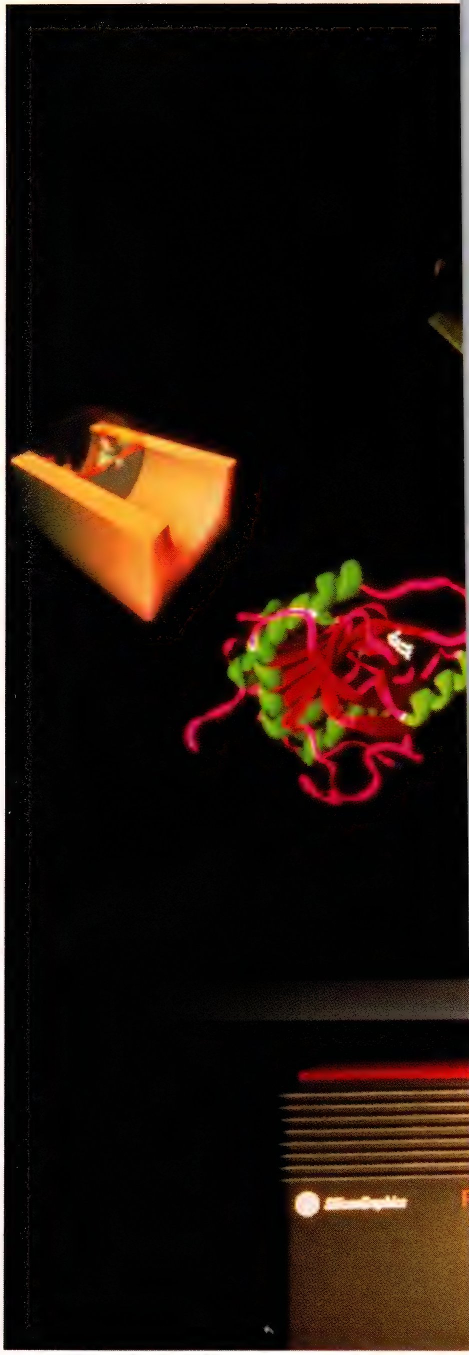
IT'S READY, AIM, FIRE! IN A SEGMENTED MARKET

Smaller work station vendors grab niches as big players hustle to stay on top

BY TOM MANUEL



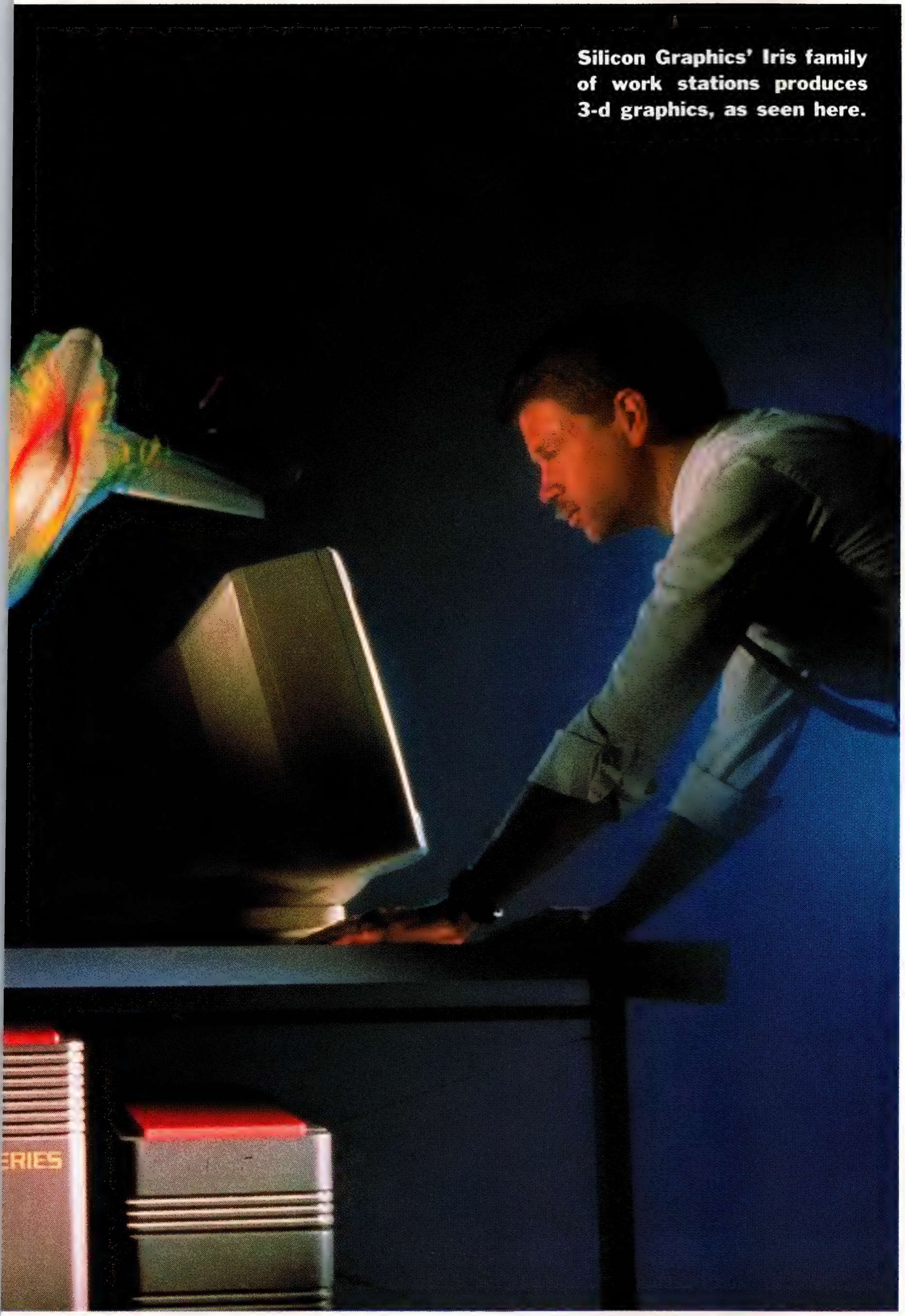
Excitement is running high in the technical work station industry. This fastest-growing segment of the computer market is seeing almost daily business developments and alliances along with very fast-paced technical and product developments. Three top vendors are slugging it out for market-share leadership as many smaller companies scramble to find a differentiated niche for themselves

Technical work stations are now big business. The market will reach a hefty $5 billion to $6 billion this year and is still growing at better than 30% a year, according to market researcher Dataquest Inc. of San Jose, Calif. Since unit prices are falling every few months, the market figures represent a tremendous number of work stations sold. And that's good news for a whole slew of companies, even beyond the work station vendors themselves. Among these vendors, three companies are preeminent: Hewlett-Packard, newly merged with Apollo, Sun Microsystems, and Digital Equipment. Besides the big three, many smaller work station makers are getting healthy pieces of the pie, as are their suppliers—vendors of application-specific integrated-circuit design systems, programmable logic devices, microprocessors, and memories, not to mention software houses. Meanwhile, perhaps the most feared competitor of all, IBM Corp., is poised for a new thrust on the market (see p. 68).

The rapid growth and strength of the work station market is an indication of the rapid acceptance of a new way to do computing—networked work stations and servers. It's a concept that has caught on fast, and one that many see as the ultimately displacing the venerable setup of shared minicomputer and terminals. Work station computing is also likely to replace at least some mainframe computing soon, if not most mainframes in the long run. Personal computers, in many cases, will become just another type of work station on the network.

"End users have embraced work-group computing solutions," says Ed Zander, vice president of corporate marketing at Sun Microsystems Inc. in Mountain View, Calif. "Sun is a computer company; we don't use the name 'work station' because we are no longer selling in a niche market called work stations. We are selling in the computer market."

Hand in hand with the popularity of networked machines is a trend toward tying work stations to existing computing resources. "There's increasing interest in how work stations fit into a company's overall computing environment, where connectivity and uptime are both very important," says Douglas Johnson, work station product manager for Hewlett-Packard Co.,


Silicon Graphics' Iris family of work stations produces 3-d graphics, as seen here.

Palo Alto, Calif. The management-information-system managers are getting involved with work stations, he observes, "another sign of the maturing of the concept."

"The customers for work stations are well identified and they've made known what they want," says Don McInnis, vice president in Digital Equipment Corp.'s Engineering Systems Group in Marlboro, Mass. And what they want, he says, includes products that are properly priced, offer good performance at the price, and fit easily into the customer's computing environment. But the list also includes matters related to the vendor's overall corporate strength, such as field service and "whether or not the vendor will be around for the long haul," McInnis adds (see p. 70).

Technically, "the driving forces in the work station market in the next two years include making a network of computers work like one virtual machine," says Mark Tolliver, marketing manager of HP's work station group. "Work station systems need to support the work of teams of people, such as a team of engineers. This will be the ultimate system."

This new type of computing originated in 1980, when startup Apollo Computer Inc. invented the first engineering work station, taking a proprietary approach with its own hardware design, system software, and networking. Apollo's arrival was followed quickly by the entry of another startup, Sun, which took a different tack. Sun adopted as many industry standards as possible, such as Unix, Ethernet, and the Transmission Control Protocol/Internet Protocol. Where standards were not yet available, Sun tried to set them, as in its Network File System, which became a de facto standard. Both companies flourished in the early heyday of work stations. Apollo, based in Chelmsford, Mass., took an early lead, but Sun caught up and then passed it.

The fortunes of both companies have suffered recently. Apollo has had problems maintaining growth and profits in the last couple of years, and was rescued when HP acquired it last April. The merged work station operations, which together lead the market with a 29% share, according to Dataquest, are moving toward combining platforms and fully embracing industry standards (see p. 68). Meanwhile, no longer is everything bright and cheery at Sun. The darling of the industry, which last year ranked No. 2 with 27% of the market, according to Dataquest, recently experienced a glitch in earnings performance. It reported a loss of $20.3 million in its fourth quarter.

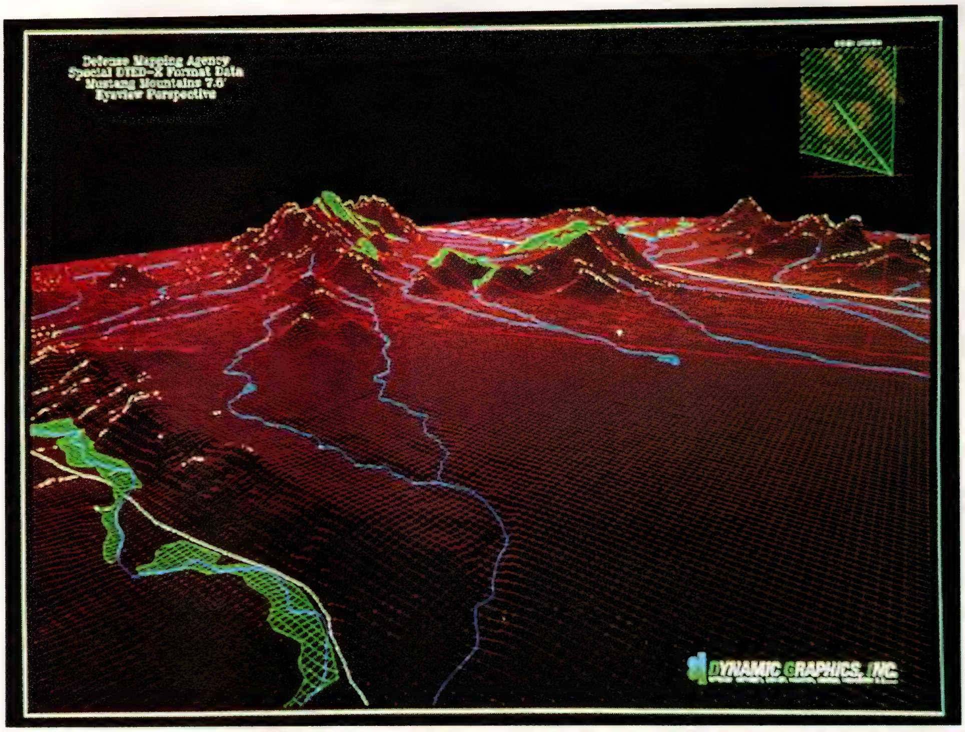
One of the chief early applications that contributed most to the work station boom was electronic design automation. Companies like Daisy Systems, Mentor Graphics, and Valid Logic Systems, all startups, created a new EDA business based on work stations and networks, which is still thriving today.

Many other applications have come to the fore since then. One of the biggest is mechanical computer-aided design. Other growing applications are desktop publishing, computer-aided software engineering, three-dimensional visualization, molecular modeling, and geographical information systems.

The growth of these applications plus new ones coming on stream all the time are fueling the growth of the work station market. Besides this flowering of new applications, "opportunities for new markets will follow better programming tools and user interfaces," says HP's Johnson. "Every vendor has major investments in making work stations easier to use." Combined with these factors is the price drop: buyers can now purchase a low-end unit for about the same price as a high-end PC.

All this has produced double-digit growth rates. Dataquest predicts a 37% rise in work station revenues in 1989 and a 30% compound annual growth rate between this year and 1993. But as the market grows larger, Johnson says, the growth rate will inevitably slow. "We will see some peaks and valleys," he says.

All vendors are scrambling for market share, with the big three fighting the most visible battle. Besides HP, Sun, and No. 3-ranked DEC, the new thrust by IBM and by vendors of high-end PCs—including Apple Computer Inc., with its Macintosh—



Megatek's Sigma creates a surface model of the Fort Huachuca, Ariz., area from digitized terrain-elevation data. Vegetation is in green, rivers in blue, and roads in maroon.

offers some additional competition. The market really has two tiers: the high-volume generic work stations, like those offered by the major vendors, and a spate of more specialized work stations going after niche application markets.

Among them are Silicon Graphics Inc.'s 3-d visualization work stations. The Mountain View-based company, which nabbed 4% of the market last year, does not expect to be a niche player for long.

"We decided early to concentrate on the [3-d visualization] sector that will dominate the market by the mid-1990s," says Ed McCracken, president and chief executive officer. "It's a small part of the market today—but we expect it to grow faster than the [work station] market as a whole."

With such smaller vendors nailing down niches and attempting to leverage them into bigger market share, today's market leaders must hustle just to stay in place, let alone move further out in front. What does it take to be successful? "The equation for success in the work station market is rapidly moving toward the equation for success in the general computer market. It's a migration," says William J. Filip, assistant general manager for advanced work stations at IBM's Advanced Work Station Division in Armonk, N. Y.

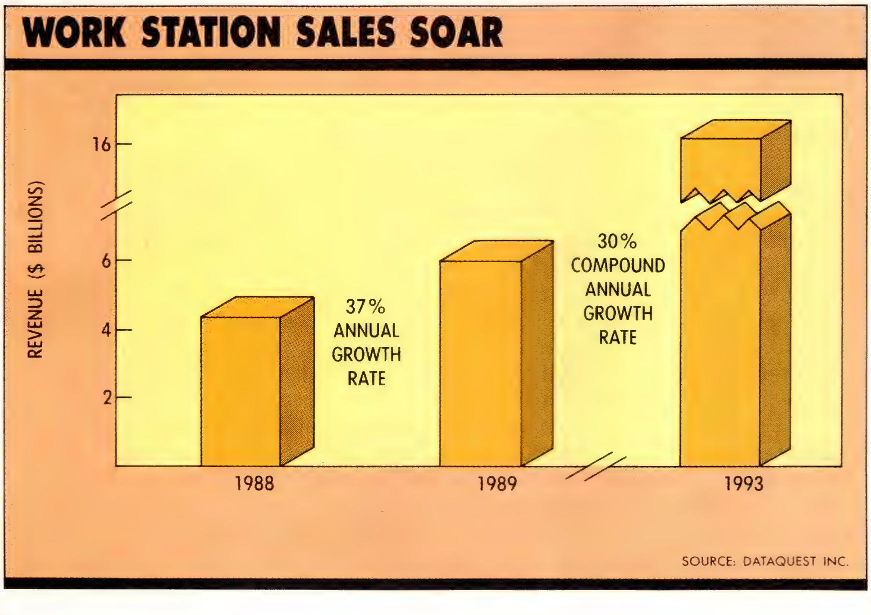
One hot area of competition is in delivering more microprocessor performance. With reduced-instruction-set-computing architectures now entrenched as the prime technology drivers for work stations, vendors are relying on enhanced RISC processors to outdo their competitors in price/performance. The result is an overheated RISC processor market [*Electronics*, May 1989, p. 70]. "It is really still early in the RISC work station wars, but the next two years should reveal which architectures will be the big winners for most of the next decade," says Micheal Slater, editor and publisher of the *Microprocessor Report* newsletter in Palo Alto. "There are plenty of decent architectures—and some not so decent architectures—to pick from, and the industry now needs to focus on improved implementations."

Silicon Graphics uses the popular MIPS processor chip sets from MIPS Computer Systems Inc. of Sunnyvale, Calif. Other companies making MIPS-based work stations include DEC, Stardent Inc. (formerly Ardent Computer Corp. before its merger with Stellar Computer Inc.), and MIPS Computer Systems itself, with its line of RISCstations. Another popular RISC technology is Motorola Inc.'s 88000 chip set. It is used in work stations by Data General, Opus Systems, Sanyo/Ikon, Tadpole Technology, Tektronix, and a European company called Dolphin Technologies. Sun's entry, its Scalable Processor Architecture, claims two vendors with products on the market in addition to Sun itself: Megatek Corp. and Solbourne Computer Inc.

Solbourne sells higher-performance clones of Sun work stations. The Longmont, Colo., startup is gaining success with its first product line, the Series 4, which was introduced last January. Already, Solbourne is upping performance dramatically with Series 5, to be introduced this month (see p. 65).

Another niche player is Tektronix Inc., which weighs in with a line of high-performance graphics work stations based on the Motorola 88000 RISC chip set. The

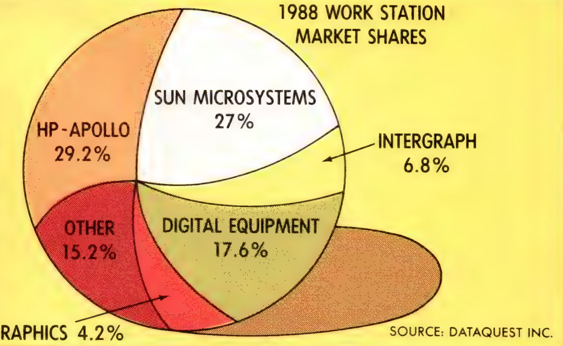
WORK STATION SALES SOAR



SOURCE: DATAQUEST INC.

HP-APOLLO LEADS THE WAY

Who is the market leader? The answer depends on which analyst you ask. Dataquest Inc. apportions market share, based on hardware sales alone, as shown at right. International Data Corp. offers rankings based on hardware, software, and consulting services. IDC places Sun first with 32.7% of those revenues, followed by HP at 29.6% and DEC at 20.9%.



SOURCE: DATAQUEST INC.

Beaverton, Ore., company's market strategy focuses on visualization and high-end graphics. "Tektronix cannot win in the generic work station business," says Pat Welch, general manager of the Interactive Technologies Division. "We have spent time trying to distinguish the Tektronix offering." The concept of visualization technology and applications using it turned out to be the key. The company will "take on the visualization market in three or four vertical markets, such as MCAD, earth sciences, and prepress," says Welch—partly with the help of a new low-end work station to be introduced this month (see p. 61).

The niche strategy taken by Tektronix is typical of many other vendors. Megatek, for example, adds very high-end 3-d graphics to work stations built around processor boards and system software from Sun. The San Diego company's Sigma 70 is the classiest graphics work station currently on the market. "Sun products plus high-performance graphics is a good combination for the markets we are targeting," says Robert Varga, Megatek's vice president of marketing. "Those target market applications are high-end CAD and visualization." Megatek also responds to customer requests for special features—about 70% of its business has a strong custom component, Varga says. Another niche is in ruggedized work stations for the military.

Opus Systems, another niche player, markets both coprocessor boards for IBM PC and compatible computers and complete work stations. Opus is in the Motorola 88000 camp. "The 88K market is exciting for us; we chose to be aligned with an industry-standard processor, and the 88K chip-set performance is remarkable," says Tom Lacey, marketing manager.

There is strong support for the 88000, Lacey says. "The driving forces of the work station market are software interchangeability, a variety of distribution channels, DOS functionality, and strong product support." The 88000 camp is strong in software interchangeability because of the organization known as 88Open Consortium Ltd. 88Open is fostering a binary-compatibility standard for interchangeable software among all 88000 systems and, toward that end, is supporting a software initiative to ease porting applications to the standard.

With regard to DOS functionality, "work stations and PCs have collided," says Lacey. "The middle ground is called the PC work station. The PC work station is a trend; Sun and DEC are both moving this way—DOS capability and DOS distribution channels."

Another new vendor in the 88000 camp is an old-line minicomputer company, Data General Corp. The Westboro, Mass., company started shipping its Aviion work stations to customers in volume in August. "One of the strong early application markets for the Aviion is the medical imaging market," says Sanford Friedman, Data General's manager of work stations. Other large market opportunities, he says, are geographical information systems, technical markets in the federal government (intelligence agencies), software development, and technical publishing. It appears that the emerging market segments for work stations are the targets for most, if not all, of the niche players.

'The next two years should reveal which of the RISC architectures wins the war'

Data General is one of the vendors with a large installed base of computers to sell to. "Another opportunity I am high on is our big installed base of 16-bit minis for real-time and lab-science applications," says Friedman. "Our RISC-based work stations with floating-point coprocessors will become much more common in this space." Other vendors with large installed bases of minicomputers and mainframes—including DEC, IBM, and HP—likewise will be exploiting them in an effort to boost work station sales. So will Tektronix, which has a good-sized installed base of graphics terminals.

Another up-and-coming niche player is Sony Microsystems Co., which has a multitiered work station strategy. "In Japan our approach is very much like Sun's approach to the business here," says Thomas L. Steding, vice president of marketing and sales. Sony is a leader in the work station market in Japan and will pursue it as a generic business. However, in the U. S., "we decided we would get further, faster if we focused on certain segments—but not exclusively," says Steding. "There will always be some generic work station business. The segments we are targeting will use Sony's strengths in certain technology areas, such as color display, video, audio, optical storage, and imaging."

The leading company in the CAD market, Intergraph Corp., has been primarily a turnkey systems vendor. Now it is offering high-end work stations based on its own RISC processor architecture, the Clipper. "Our fast Clipper, the second generation, is doing very well," says William D. Zarecor, vice president of marketing at the Huntsville, Ala., company. Two versions deliver 10 and 14 million instructions per second, respectively. "We will be delivering a 20-mips Clipper 300 plus a server product in the fourth quarter," Zarecor says. Intergraph has almost 7% of the work station market, according to Dataquest. "We expect to improve on that," Zarecor says.

A company that is backing into the work station market with a unique niche is Symbolics Inc. The Burlington, Mass., company is known for its technology in artificial intelligence and symbolic processing. It has developed a tagged-architecture processor known as Ivory that does efficient symbolic processing. Now the company is putting together a coprocessor board that, with its extensive software, turns Sun machines and Macintoshes into symbolic processing work stations for software development and deployment. With the new UX400S board plus Symbolics software, users can integrate very tightly with the Sun system. ☐

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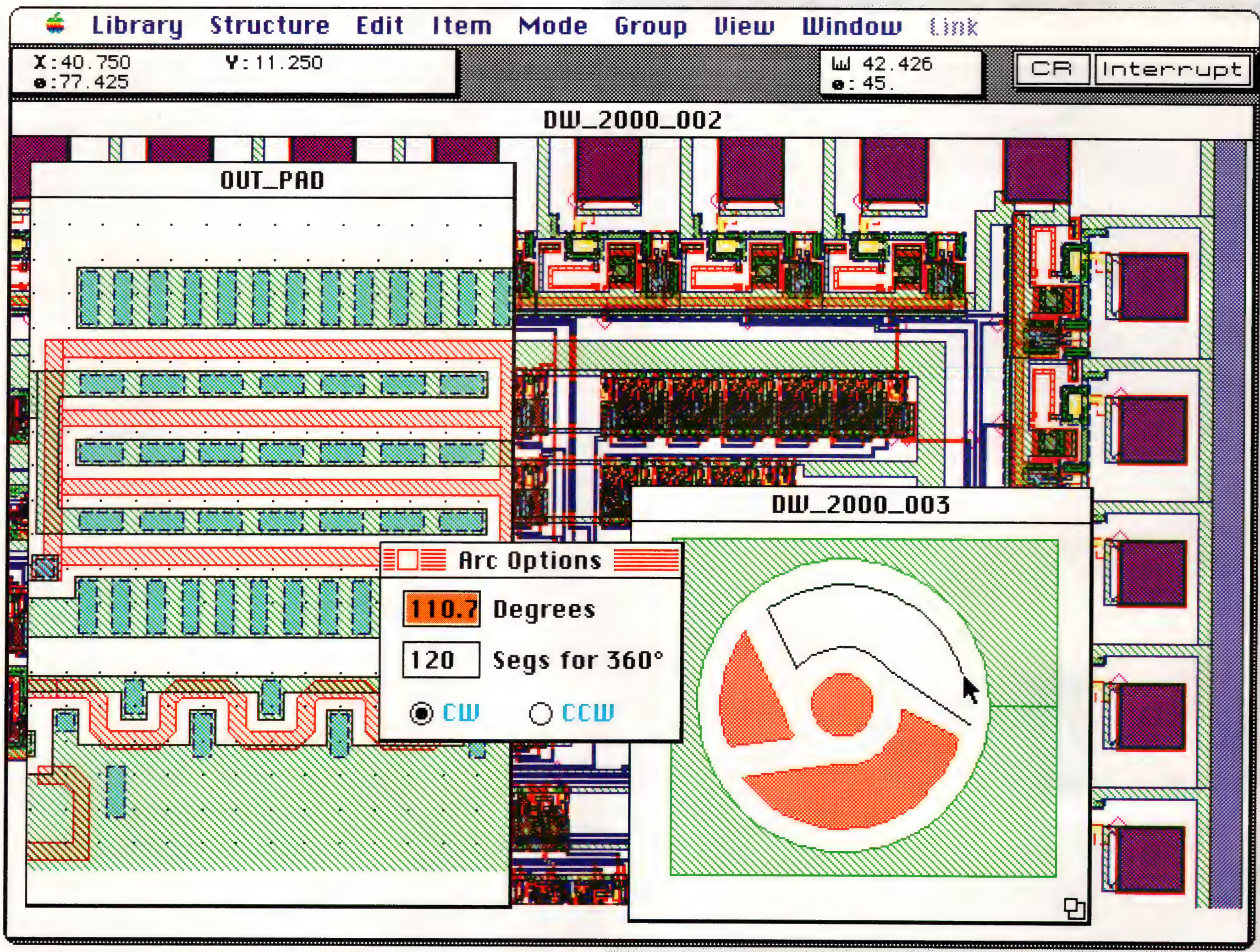

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At $3,990, Apollo's new 68030-based Series 2500 is priced about the same as a personal computer

With the help of four ASICs, Apollo's Series 2500 delivers up to 4 million instructions/s.

Despite the energy devoted to managing the six-month-old merger of the Apollo Division into Hewlett-Packard Co. (see p. 68), there's no sign of a slowdown in product development in the two ogranizations. Each of them last month took the wraps off new work stations, with Apollo becoming the first work station vendor to crash through the $4,000 price floor with its Series 2500 machine.

Apollo also unveiled the Desktop Visualization System (DVS), a two-board set that greatly boosts the vector- and polygon-drawing performance of Apollo's year-old Series 3500 and 4500 units. And parent HP hit the street with a high-performance graphics unit built around the company's reduced-instruction-set-computing Precision Architecture.

The Apollo Series 2500 combines a 20-MHz Motorola 68030 processor with Apollo-designed application-specific integrated circuits to deliver integer performance of 3.5 to 4 million instructions per second. A diskless model with 4 Mbytes of memory sells for $3,990. It competes with the VAXstation 3100 from Digital Equipment Corp. and the Sun 3/80 from Sun Microsystems Inc., says Robert Weinberger, director of systems product marketing at the Chelmsford, Mass., division.

The Series 2500 with a 15-in. monochrome screen would go up against a 3-mips diskless VAXstation 3100 with a similar screen selling for $7,250, he says, although the DEC unit has 8 Mbytes of memory. The nearest Sun 3/80 runs at 3 mips and has the same-size memory but a 17-in. monochrome screen; it sells for $5,995.

The ASICs in the 2500 help hold the price down by minimizing the parts count, allowing Apollo to fit the unit on a single motherboard. One of the ASICs is the controller for a Small Computer Systems Interface, which can accommodate two internal 200-Mbyte disk drives plus external mass storage up to a total of 2.3 Gbytes.

The 2500 has no trouble reaching 3.5 mips, versus the 1.5-mips integer performance of Apollo's 68020-based Series 3000, which it replaces. Weinberger says the 2500 will probably be rated at 4 mips. Its floating-point performance—0.246 (single-precision) or 0.203 (double-precision) million floating-point units per second for the Linpack benchmark—is 2.5 times better than that of the Series 3000.

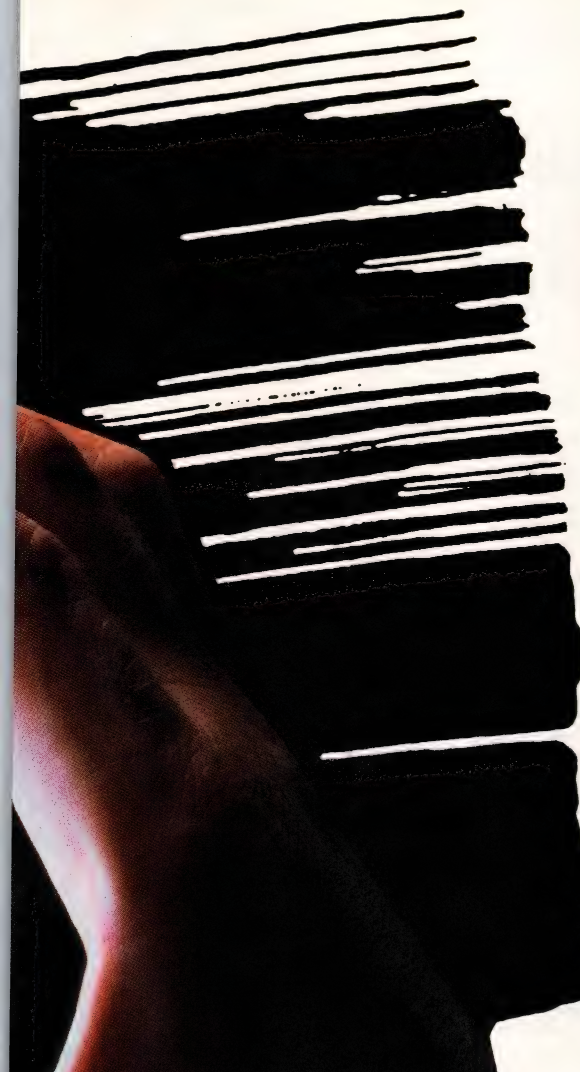
To boost graphics performance of 3500 and 4500 units, Apollo has come up with the two-board DVS, which can be installed as a field upgrade. One board is a transformation processor, the other an image memory or frame buffer that offers 1,280-by-1,024-pixel resolution in 8- or 40-plane versions. Together, they add a lot of graphics clout.

For example, a 3500 with no graphics accelerator option can draw 6,000 three-dimensional vectors/s; using a 40-plane DVS (24 planes of image memory), the speed rockets to 290,000 3-d vectors/s. For a DVS-equipped Series 4500, the boost is from 9,000 to 300,000 3-d vectors/s.

For solids modeling, a 40-plane DVS-assisted 3500 work station draws 15,000 3-d polygons/s; a similarly equipped Series 4500 does 20,000/s. That compares with about 5,000 polygons/s for the nearest competitive work stations from DEC and Sun, says Jan Carl Silverman, group manager for graphics products at Apollo.

Silverman says two chips are the key elements of the transformation-processor. The 2-d/3-d transformation engine itself is an available floating-point chip rated at 24 megaflops. (Apollo declines to name the chip's maker.) The drawing engine is a 100,000-gate CMOS array designed by Apollo. The DVS option adds from $7,500 to $15,500 to the price of a Series 3500 or 4500.

Meanwhile, back in Fort Collins, Colo., HP's Workstation Group hasn't been sitting on its hands. Its latest entry is intended for two-dimensional graphics tasks. Called the HP 9000 Model 834CH, the unit employs HP PA, the firm's approach to RISC, to deliver 14-mips integer performance and 2.02 megaflops. With a 16-in. color screen, the price is $19,375; a 19-in. color version sells for $22,500. Its performance puts it in a class with DEC's 14-mips RISC-based DECstation 3100, which, in a 19-in. color version, sells for $5,000 less. ☐



Sizing Up the Earth in 200 B.C.

Eratosthenes believed the earth was round. As director of the great library at Alexandria in Egypt, he decided to go beyond abstract argument and actually measure it to back up the argument.

Eratosthenes

Knowing that the midsummer noon sun shone straight down a vertical well in Syene far to the south, he measured the slight angle of the sun's shadow in Alexandria on the same day. He figured the distance between the two cities by how long it took a camel to walk there. Then, with a little simple geometry, Eratosthenes came up with fairly accurate figures for the earth's circumference and radius. His pioneering measurement made a significant impact on history.

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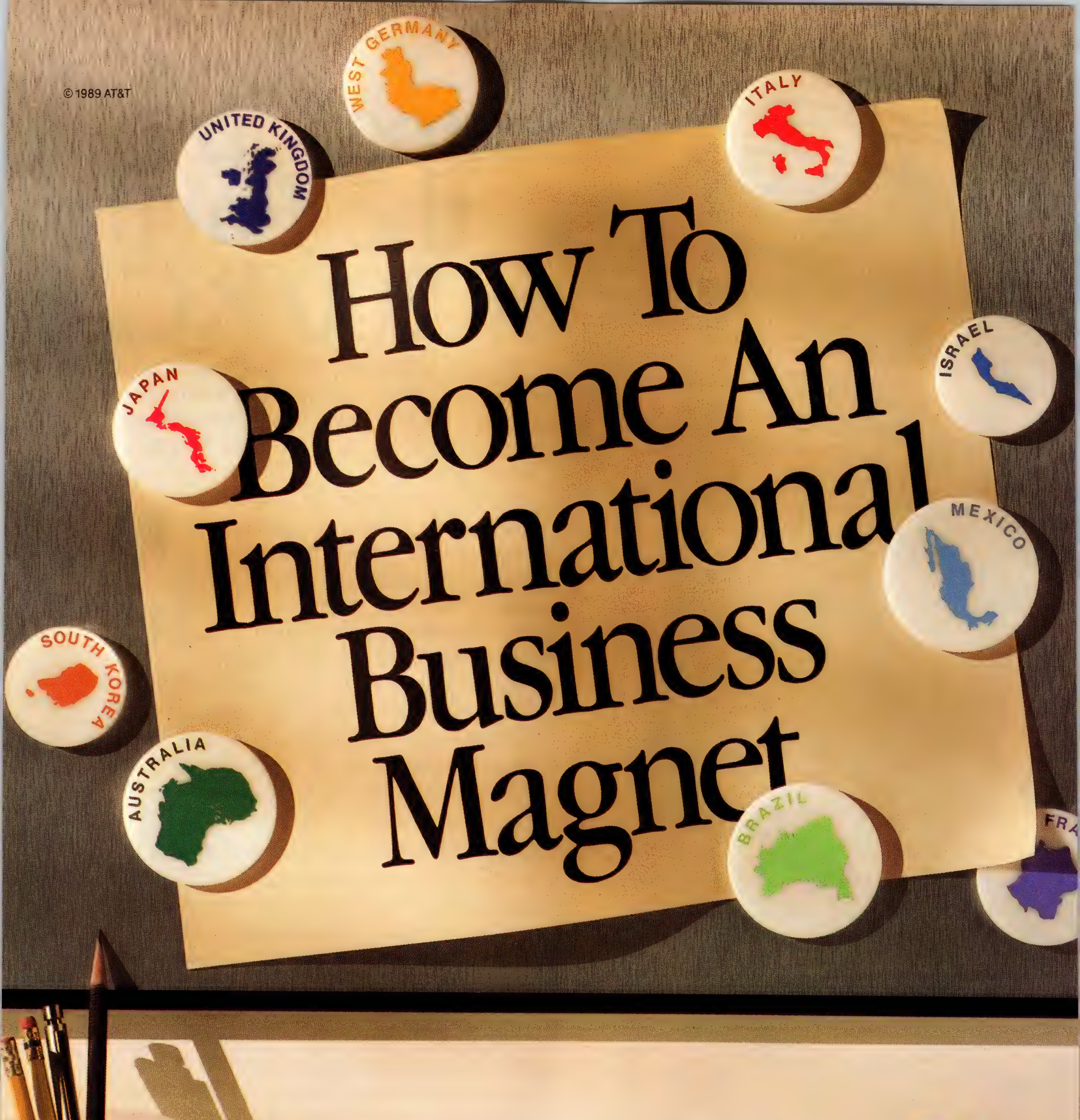

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MORE MIPS FOR THE MONEY

BY JONAH McLEOD

Tektronix seeks visibility in the work station arena with a machine that gives hot graphics at a low cost

The XD88/10 offers color graphics and 17-mips performance for $15,000.

Tektronix Inc. is not a name that immediately leaps to mind as a vendor of high-performance work stations. But the Beaverton, Ore., company wants to change that. Tektronix believes it can leverage its expertise in graphics terminals to make a name for itself in the fast-moving work station market.

At least one market watcher thinks the company will succeed. Mike Tyler, director of graphics and imagery at Dataquest Inc. in San Jose, Calif., predicts that Tektronix will garner enough market share to be among the top five suppliers in the near term. One reason Tyler is so bullish on Tektronix is its latest work station, the XD88/10.

At $900 per million instructions per second, the machine sets the price/performance pace in the industry, says Scott McCowan, Tektronix's marketing manager for the XD88/10. By comparison, he says, Sun Microsystems Inc.'s new SparcStation 1, a similarly equipped machine, comes in at over $1,000/mips.

Due to ship in November, the Tektronix machine gets its high performance using a 20-MHz 88100 reduced-instruction-set microprocessor from Motorola Inc. of Austin, Texas. The unit incorporates a graphics feature called Color Cache, which gives it color graphics performance equivalent in resolution to a monochrome work station at a price four to eight times less than a full-blown color graphics accelerator, McCowan says.

The XD88/10 represents the low end of Tektronix's line of Motorola 88000-based work stations, introduced in April. These machines are an outgrowth of the company's graphics terminal products, introduced in the early 1970s and still actively marketed by Tektronix.

Entering the work station fray means taking on such heavy hitters as Digital Equipment, Hewlett-Packard, IBM, and Sun Microsystems—companies that have significant head starts on Tektronix. McCowan concedes that the competition is stiff, but he believes that Tektronix's reputation as a graphics-terminal leader will help it compete. "Applications that traditionally used Tektronix terminals typically run on mainframes or some other distant host," he says. "The customer sees the Tektronix terminal, not the host driving the terminal, and is more familiar with Tektronix hardware."

Analyst Tyler agrees. "The vendor with the best graphics will get the business in this customer base," he says. "Tektronix has as much name recognition as DEC and has the stronger graphics capability." Last year, Tektronix accounted for a mere 0.9% of the $4.1 billion work station market, but Tyler believes the company can boost that share to 3% to 4%, pulling it alongside Silicon Graphics Inc. in the top five.

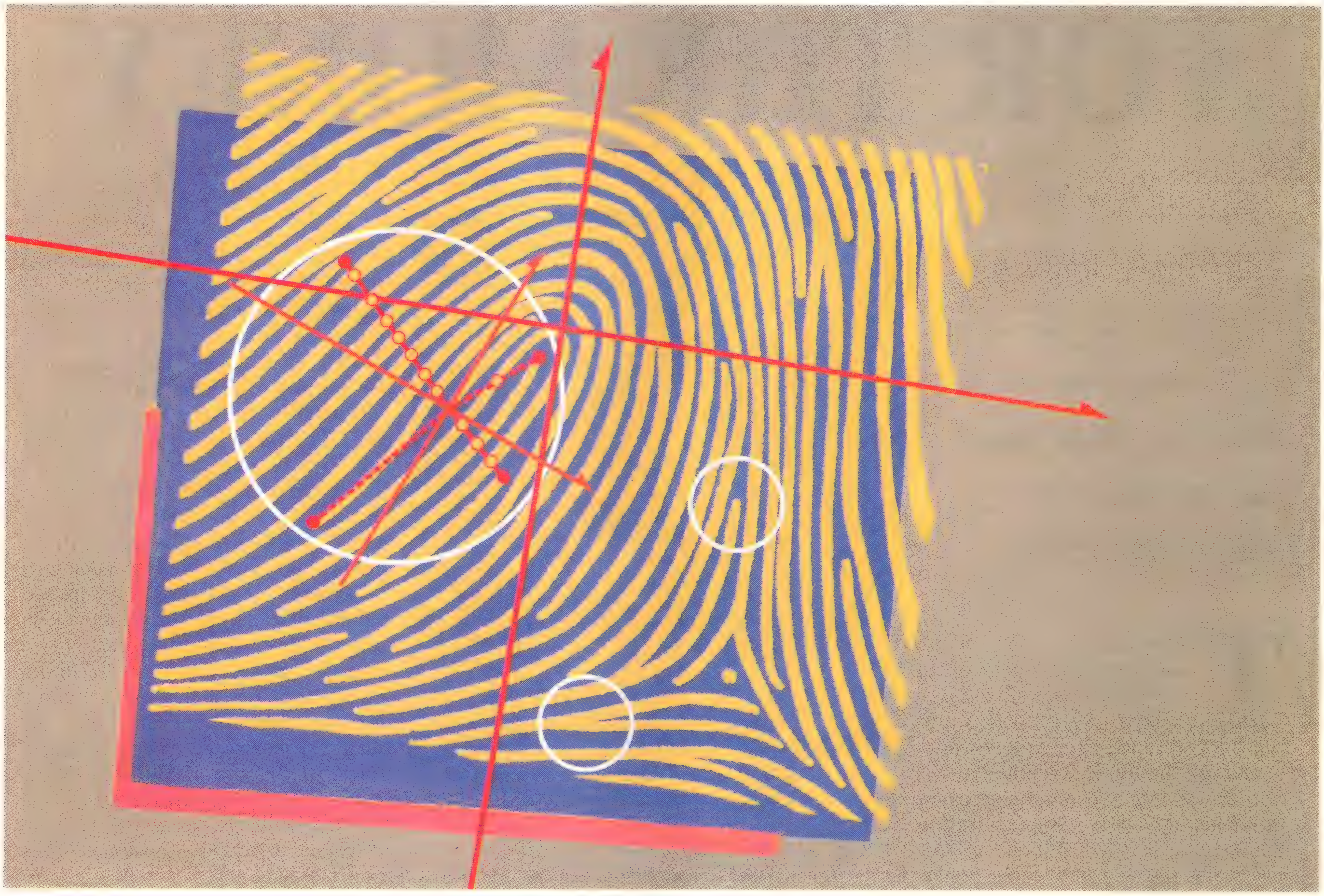
Tyler says the XD88/10 will be critical to Tektronix's success. "The idea behind a work station is low-cost networked computing," he says. "Customers want to buy 20 to 30 work stations, of which maybe 20% will be high-end units with the rest being low-end systems. Until now, Tektronix had a high-end solution but lacked the low-end offering to attract buyers."

Priced at $15,000, the 17-mips XD88/10 offers price/performance numbers that outpace competitive offerings, Tyler says. The color SparcStation 1 GX, the Apollo 3400/3500, and the DEC 3100 sell for $15,000 to $17,000, while Silicon Graphics' Personal Iris costs $21,000; these machines offer only 12 to 14 mips.

The XD88/10 offers a screen resolution of 1,280 by 1,024 pixels, which exceeds that of some competitors. It features 8-bit planes expandable to 24 bits; among the competition, only the Personal Iris is expandable to 24-bit planes. Tektronix and Silicon Graphics are the only two vendors offering a VMEbus slot, a plus for those users wanting to expand the system with the large base of VME add-on cards.

The Color Cache feature consists of a proprietary gate array that performs high-speed bit manipulation. Four of the arrays provide an interface between the work station's 32-bit VMEbus and the 256-bit pixel data bus. This bus attaches to the 8-bit-plane frame buffer that drives the color graphics display. In the Color Cache scheme, the work station's central processing unit stores the colors in use—32 of a possible 256 colors, with 8 bits per pixel. As long as the image requires one of these 32 colors, the CPU can specify the color with a single bit. If another image displayed on the screen requires a different set of colors, the CPU must reconfigure the cache. ☐

NEC NEWSCOPE



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NUMBER 142

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NEC's new Nd: YAG laser (YL117-6C) is also setting output power records: 2.1kW in CW mode, and 2.4kW in quasi-CW mode. Output is stabilized by switching regulator power supplies which also permit high speed pulse modulation.

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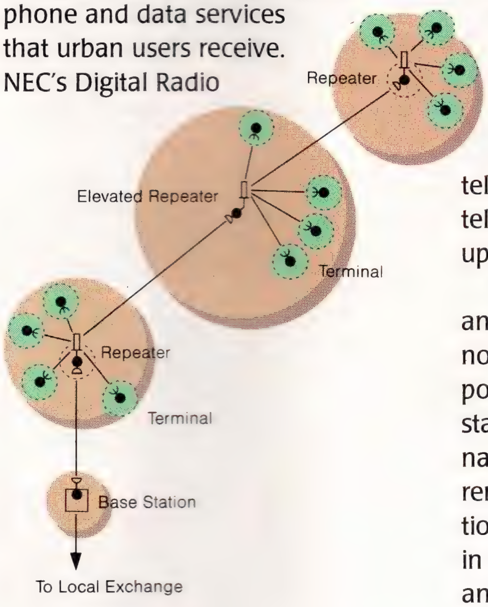

DRMASS is a highly economical point-to-multipoint microwave system using TDM/TDMA (Time Division Multiple-Access) technologies. It covers a radius of approximately 600km with typically 11 repeater stations. Each repeater serves a 20km-radius cell. A DRMASS network with 4Mbps transmission capacity (60 time slots) and demand-assigned multiple-access/concentration systems can accommodate up to 1,024 subscribers. In addition to telephone services, DRMASS offers telex service and data transmission up to 64kbps.

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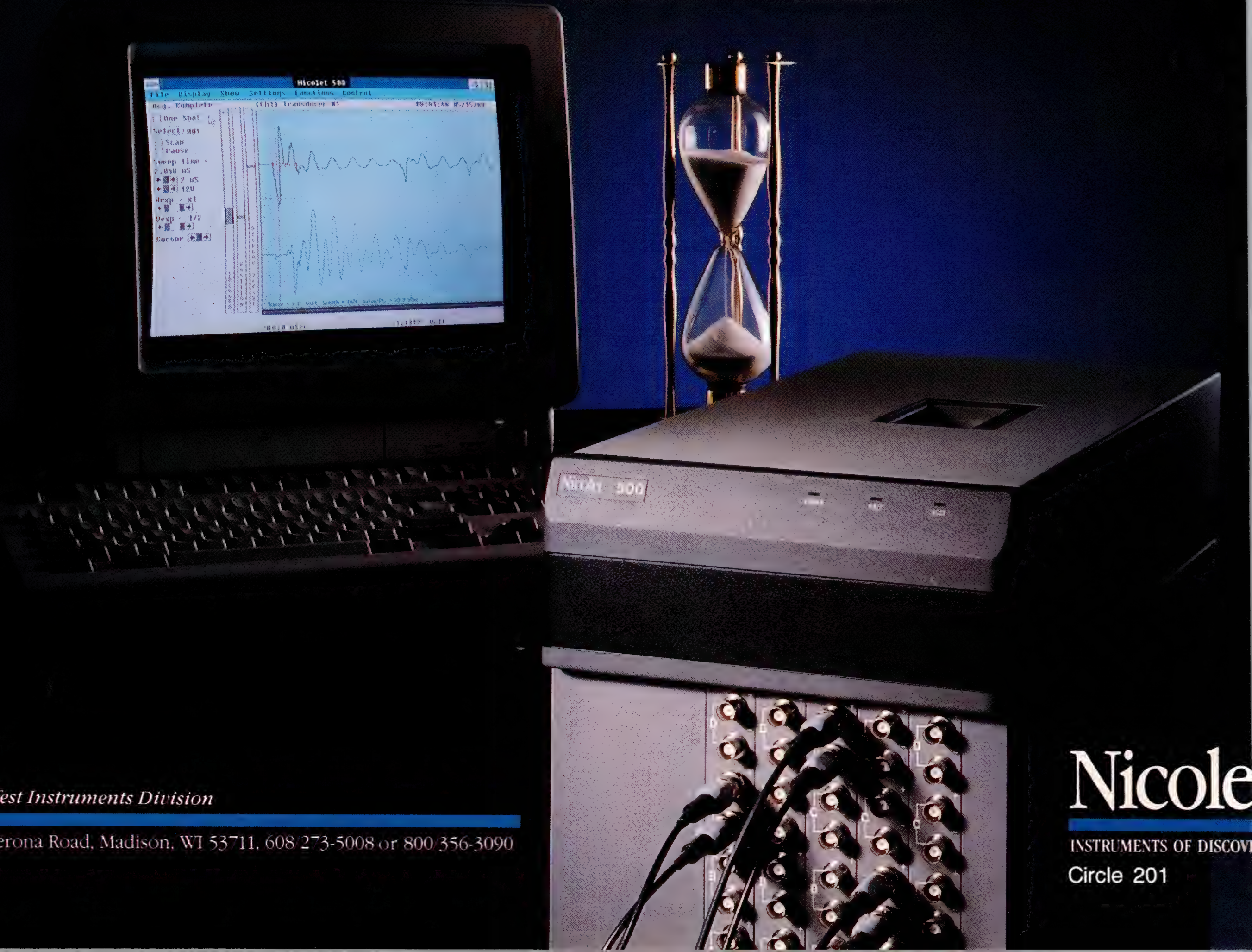

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Circle 201

ANOTHER COUP FOR SOLBOURNE

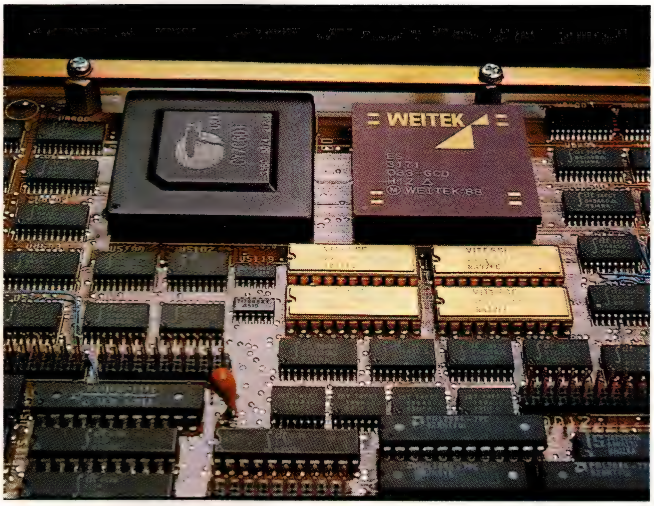
BY TOM MANUEL

The brash startup that brought the first Sun Sparc work station clones to market has done it again. Just 10 months after it started shipping its work stations, Solbourne Computer Inc. has unveiled its second-generation machines—a line that sets the new standard for general-purpose work stations.

The Longmont, Colo., company's Series 5 central processing unit offers more than double the performance of the first-generation Solbourne Series 4. The Series 5 employs several advanced technologies to achieve 22 million instructions per second in a single-processor configuration and up to 65 mips in a four-processor setup, making it the top-performing general-purpose work station on the market. The Series 5 CPU board is available in new work stations and as a field upgrade for Series 4 products.

Solbourne was the first company after Sun Microsystems Inc. of Mountain View, Calif., to bring a Scalable Processor Architecture product to market. Sun, which originated the Sparc reduced-instruction-set computer scheme, made Sparc an open architecture by licensing the chip design and the Sun operating software. Although several work station makers have licensed Sparc and announced plans to offer products, Solbourne remains the sole supplier of Sun-compatible Sparc equipment.

Among the advanced technologies used in the Series 5 is the CPU. The Solbourne machine is the first product to contain the 33-MHz CY7C601 integer CPU from Cypress Semiconductor Corp. of San Jose, Calif. It's also the first Sparc computer to employ Weitek Corp.'s new Abacus 3171 floating-point coprocessor, which was designed to support the Cypress 7C600 CPU family. Weitek's coprocessor integrates the floating-point data path and controller on one CMOS chip. Abacus chips come in 25-, 33-, and 40-MHz versions; Solbourne uses the 33-MHz part to match the Cypress CPU in the Series 5.



Powered by a 33-MHz Cypress Sparc chip, the Solbourne Series 5 CPU board blazes away at 22 mips

With the Weitek coprocessor, the Series 5 offers up to 3 million floating-point operations per second (double-precision Linpak megaflops) in a uniprocessor work station and up to 8.9 megaflops in a four-processor configuration.

In another technology coup, the Series 5 is the first work station to employ high-speed gallium arsenide circuitry. Solbourne's engineers selected GaAs input/output random-access memories from Vitesse Semiconductor Corp. of Camarillo, Calif., to create a fast physical cache memory—the first purely physical cache in a Sparc design.

A physical cache is much better suited for maintaining cache consistency in multiprocessor systems than the virtual cache used in earlier Sparc designs, including the Series 4. "The overhead associated with maintaining cache consistency in a multiprocessor system made using virtual cache very difficult," says Nick Mati, Solbourne's founder and engineering manager for the Series 5 board. The Series 5's 128-Kbyte physical cache replaces the 64-Kbyte virtual cache used in the Series 4.

With a physical cache, all processors in a multiprocessor system can work with identical data addresses, something that can't be done with a virtual cache. By eliminating areas of data contention—hot spots in the cache—a physical cache improves system performance.

Making all these advanced technologies work efficiently requires a fast advanced bus system. Solbourne uses a high-performance dual-bus system: a 64-bit K-bus system bus for multiprocessing support and a VMEbus for robust I/O activity. This bus structure, designed for the initial Series 4 work stations, offers enough capacity for faster generations of processors and cache memories, such as the Series 5 upgrade.

Solbourne is using Series 5 boards in several models of work stations and servers. Solbourne offers six server models ranging from single-processor 22-mips machines starting at $33,400 all the way up to a 65-mips, 64-Mbyte, four-processor model at $172,600.

In work stations, Solbourne offers two desktop models, a single-procesor machine at 22 mips and a dual-processor model at 40 mips, priced from $31,900 to $62,200. Four desk-side work station models are also available, with one to four processors. They run at 22 to 65 mips and are priced at $45,400 to $122,400. ☐

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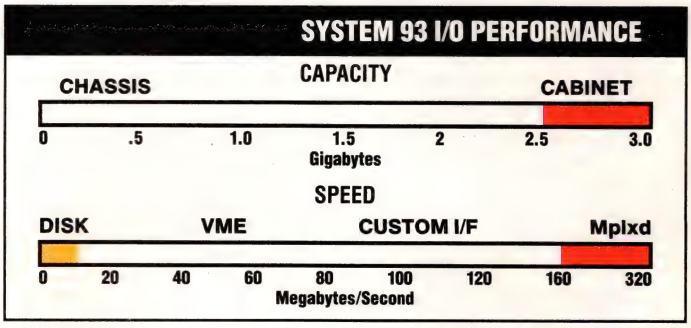

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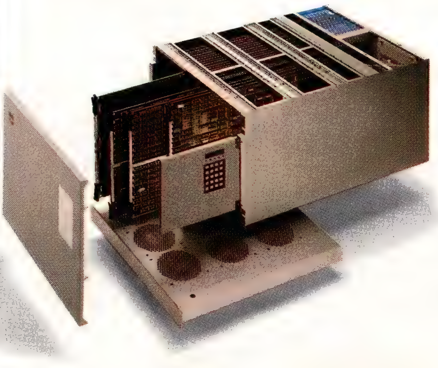

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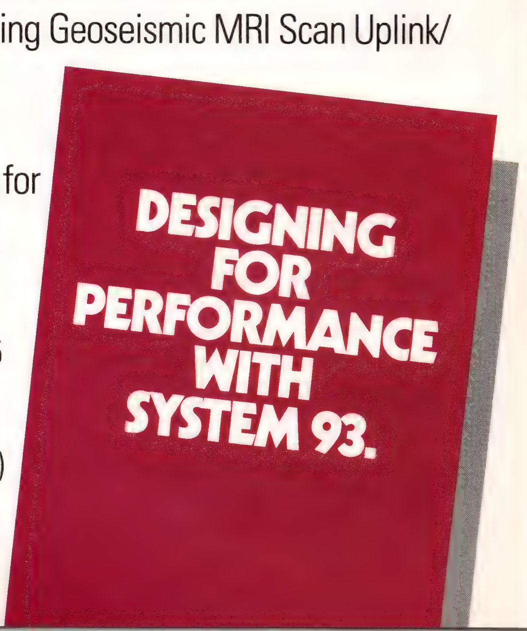


Circle 229

MAPPING OUT

It's no easy job mounting a coherent offensive in today's work station business. Here's how three companies with big stakes in the marketplace—IBM, Hewlett-Packard, and DEC—are doing it

IBM

The world's largest computer company is getting ready for a new assault on the work station market. IBM Corp. is hoping to gain some ground on its trail-blazing competitors with the third generation of its RT line of reduced-instruction-set machines, to be introduced late this year or early next.

The new machines "will have a significant architecture change to get [more] floating-point performance," says Bill Filip, assistant general manager for advanced work stations. IBM will also add input/output extensions and push graphics capability beyond that of the current-generation RT, which has been a disappointment in the marketplace.

Officially, the Armonk, N. Y., company has issued the usual disclaimer about unannounced products. "We do not have a new announced product in the work station market," says Fillip. Rather, "we have been disclosing some information about our next-generation work station family to certain customers and business partners as confidential information." At the same time, Big Blue is being more forthcoming than usual about the general direction it is taking with the next generation. The company hopes the new RT will boost its work station market share beyond the meager 2.7% attained last year.

Although industry watchers expected a mid-October introduction, IBM is now telling analysts the new line will not debut until January or February, says Vicki Brown, director of systems research at International Data Corp., the Framingham, Mass., research firm. "We want to get a certain number of software industry endorsements lined up," says Filip, so "the time frame [for this announcement] is late this year or early next year."

Analyst Brown believes IBM was delayed "because they haven't gathered the [application] software support." She says IBM's recent $5 million deal with Valid Logic Systems Inc. of San Jose, Calif., to develop RT software essentially represents pump-priming, because IBM will make sure that RT software will run on the new machines when they arrive. Apparently, the new machines will not be binary-compatible with the current generation, says Michael Slater, editor and publisher of the *Microprocessor Report* newsletter, so RT users will have to recompile their programs.

With the new machines, Filip indicates, IBM will be leveraging its mechanical computer-aided-design strengths into computer-aided software engineering and CAE. "This [CASE and CAE] is for the next platform," he says.

Together these three segments represent the largest chunk of the work station application market. Historically, IBM has been strong in MCAD with its mainframes and terminals, and some of that business is migrating to work stations. As this happens, IBM's market share will increase, apportioned between the RT line and the high-end Personal System/2 machines, which are considered work stations.

Another area of capability being targeted by IBM is interoperability between work stations and the other IBM products. "We will have high interoperability between Unix and Systems Application Architecture," says Filip. SAA is IBM's technology for making software compatible across product lines.

In designing the new work station line, two areas are of prime concern, says Filip—boosting the price/performance ratio and adding graphics clout. "The key focus is on a floating-point unit and advanced graphics," he says.

Thanks to the architectural improvements, the new product will have "a much higher performance level" than the current RT, he says. "If you look at the RT in the technical computing environment, it has not been well-suited for floating-point operations. It has lesser floating-point-unit capability than others in the market." (IBM declines to publish specific performance ratings.) And although the RT has pretty good graphics capability, it is not as broad as it should be to compete across a range of applications, Filip says.

In addition, "To balance the compute power with I/O capability, expect us to enhance the I/O capability on the next generation. We will use the Micro Channel as the I/O channel of the system, so you will see a Micro Channel Architecture work station family from IBM spanning 386/486 systems [at the low end] up to high-end next-generation RT RISC architectures." *–Tom Manuel*

HP

The acquisition of work station pioneer Apollo Computer Inc. isn't the only feather in Hewlett-Packard Co.'s corporate cap. In recent weeks, the Palo Alto, Calif., computer giant has made other moves to establish itself as a leader in the work station market.

For example, HP's recent pact with Hi-

A STRATEGY

tachi Ltd. of Tokyo brings it state-of-the-art chip technology for future versions of the HP Precision Architecture. The manufacturing license it gave Samsung Electric Co. Ltd. of Seoul, South Korea, supplies it with high-volume manufacturing of HP PA chips. Each initiative will help HP compete in a computer market where gross margins have steadily declined in recent years and even giants are having to change the way they do business.

With the Apollo merger, HP leapfrogs Sun Microsystems Inc. and Digital Equipment Corp. to become the paramount work station supplier in the U. S., with an estimated 29% of the market. "Before acquiring Apollo, we had decided that having a strong position in work stations was critical to our long-term overall computer strategy," says Bill G. Kay, general manager of HP's work station group. "We decided that acquiring Apollo would be one of the best ways to improve our position."

The acquisition brings HP more than just market share. To compete today, a supplier needs a substantial number of application programs running on its platform and a good-sized base of loyal customers, says analyst Joseph Payne of the investment firm Alex. Brown & Sons in Baltimore. The Apollo platform gives HP a large number of mechanical computer-aided-design application programs, something it does not have on its own platform. HP also gets major OEMs such as Mentor Graphics Corp., the leading CAD/CAE company, and Apollo's considerable customer base.

Then too, Apollo brings its Prism RISC architecture incorporated in the DN10000 work station, which addresses a shortcoming in HP's own RISC scheme. Kay concedes that the HP PA represents compromises the company made in favor of general data processing over scientific processing. "By marrying the Prism architecture acquired from Apollo, which was designed for scientific and engineering processing, with the HP PA, we easily remedy the shortcoming," he says.

Kay says another plum from the acquisition is Apollo's network software capabilities, which are particularly attractive to customers. "For example, it is possible to support 30 different network nodes with one system administrator," he says. "Other work station vendors, including HP, fall short of this number." In addition, he says, the Apollo network system is very flexible, and connecting a node is simple.

The Apollo acquisition was just the start, says Bill Kay, HP's work station manager.

But one thing Apollo didn't bring was access to cutting-edge process technology. And in the view of analyst Payne, HP's RISC architecture is beginning to run out of gas. That's where Hitachi fits in. The deal licensing the HP PA to Hitachi was not to foster a clone strategy, says Kay. Rather, "we wanted to find partners that would provide us significant competitive leverage." Through Hitachi, HP expects to have a high-end chip set much sooner than it could have developed one itself, Kay says.

The two companies will produce an architecture called PA Plus, according to the *Microprocessor Report*, a monthly newsletter based in Palo Alto. This enhancement of the original PA will contain features from Apollo's Prism. Payne questions whether the chips will arrive soon enough. The due date is 1991, and Payne wonders whether the HP PA can carry the company until then.

HP has been tweaking its process, tuning the design, and improving the operating system to wring more performance from the HP PA; the retooled version is being used in a new minicomputer, the Series 960, which boasts 40% better performance than the preceding Series 950.

Kay believes that the emphasis on raw computing power of the central processing unit is becoming less of a factor for buyers choosing one work station over another. Ensuring higher throughput—for example, by better matching a system's input/output performance to its CPU performance so that applications run faster—is becoming more important than how many million instructions per second the CPU can churn out, he says.

As the Hitachi relationship gives HP a source of high-end chips, the deal with Samsung gives it access to a low-end chip set. "Samsung is an aggressive, cost-oriented integrated circuit supplier that also has state-of-the-art IC technology," says Kay. "We expect to leverage from this relationship a low-cost chip set to build low-end HP PA products." Kay says HP will periodically form alliances with other partners for similar reasons.

Both the Apollo acquisition and the two new partnerships address the competitiveness issue that faces HP and other computer industry players. Computers and, more recently, work stations have become commodities sold at a market-dictated price, says analyst Payne. The catalyst for this major shift is open systems:

the personal computer and Unix-based work stations. "Traditional computer vendors locked customers in with proprietary operating systems," says Peter Musser, senior vice president at Regan McKenzie, an investment house in Seattle. He says these companies once commanded gross margins of 60% or more. By comparison, he says, Sun has learned to live on gross margins under 50%.

In fact, Payne asserts that HP's gross margin has fallen below 50% in recent quarters. He believes the pressure will continue as the company increases research and development spending to digest Apollo and to create new products.

While Kay would give no figure for HP's gross margin, he says the company is mindful that the work station business must be managed differently from the general computer business of several years ago. "That in no way implies that a manufacturer has to give up acceptable margins," he says. *–Jonah McLeod*

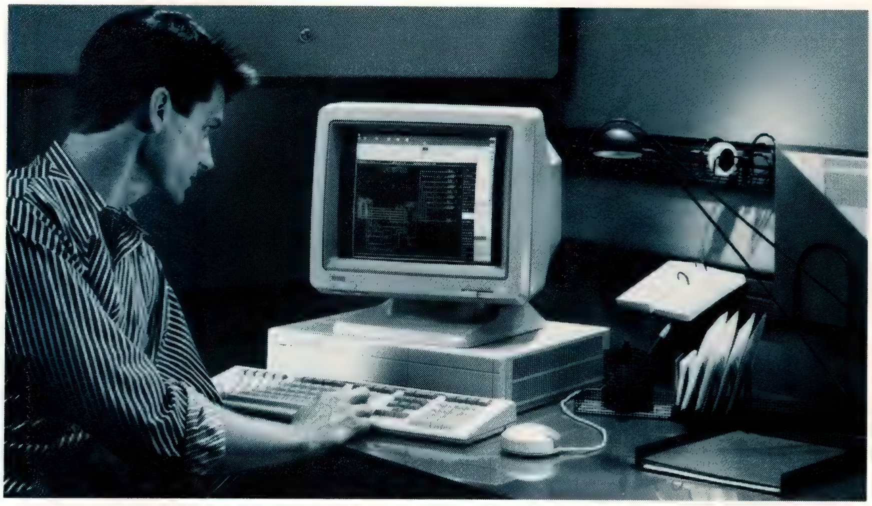
DEC

The strategists behind Digital Equipment Corp.'s aggressive push into work stations won't say when they'll achieve their goal, but they leave no doubt about what it is: to become the market-share leader in this fastest-growing segment of the computer industry. The smart money isn't betting against that happening as early as 1991. The main immediate target for DEC—now ranked No. 3 by Dataquest Inc., the San Jose, Calif., market researcher—is the No. 2 player, Sun Microsystems Inc. of Mountain View, Calif.

With a number of of product announcements since the beginning of the year, including its first reduced-instruction-set-computing work stations, DEC has thrown down the gauntlet to competitors. The $12.7-billion Maynard, Mass., computer giant held the No. 2 spot until the merger of Hewlett-Packard Co. and Apollo Computer Inc. catapulted HP-Apollo into the catbird seat. DEC says its growth rate is faster than Sun's or HP's; "it's only a matter of time before we overtake them," says Don McInnis, vice president in DEC's engineering group. Domenic LaCava, vice president for low-end systems, projects that the desktop will account for $60 billion in 1991 sales industry-wide, representing 40% of all computer revenues. "Our goal is to win the desktop," he says.

They may just make it, says Vicki Brown, director of systems research at International Data Corp. in Framingham, Mass. "Digital is extremely aggressive on price points, which is unusual for them," she says. "They've come into the market with a strategy to win." She foresees DEC overtaking Sun "probably in 1992," mainly because it takes 18 months after a RISC product is introduced to gain a sufficient base of application software to support brisk sales.

DEC's rise is remarkable considering that "two years ago, you wouldn't have found us on any [work station] market surveys," McInnis says. As a latecomer, DEC's base in work stations was built on its proprietary VAX/VMS products. But this year the company opened up its architecture with a fast-growing stable of RISC desktop platforms running the Ultrix version of the Unix operating system. Although DEC will continue to support VAX/VMS, future growth will undoubtedly be heavily RISC-based.



With a number of product announcements this year—including the low-end DECstation 2100—DEC makes no bones about its aim: to overtake Sun.

To date, the company's products include the DECstation 2100 at the low end and the VAXstation 3540 at the high. At the time the 2100 was unveiled [*Electronics*, August 1989, p. 28], it was the lowest-priced color work station on the market at $11,450. The VAXstation 3540, a two- and three-dimensional graphics platform, carries an entry-level price of $49,950. In between those two machines are at least six other work stations and various servers, some of which offer the option of running VMS or Ultrix, or both.

DEC is accustomed to competing with HP in technical minicomputers and willingly accepts the Apollo-HP challenge in work stations. Nor is it a stranger to butting heads with IBM Corp., so McInnis and Donald Gaubatz, DEC's Workstation Group manager, aren't apprehensive about Big Blue's apparent imminent push into the work station arena. "There doesn't appear to be strong customer pull for IBM work stations in technical markets," which have always been a DEC stronghold, he maintains. "Because of that, they're not likely to get much third-party software support."

But Sun is the main target right now. With a product strategy strongly based on the RISC-Unix combination that Sun pioneered, a head-on clash seems assured. The strengths that McInnis and Gaubatz cite in the run with Sun include the price/performance figures for DEC products; the choice of RISC or VAX technology and two operating systems; a strong X Windows capability, in the form of DECwindows; and other factors, including corporate strengths, that might tip the scale toward DEC in a given buy. For example, McInnis says that DEC's worldwide service organization, which he claims consistently gets top ratings in customer-satisfaction surveys, could help lure buyers.

Also differentiating DEC, says McInnis, is its Network Application Support software, an approach to multivendor computer integration that goes well beyond Sun's Network File System. "NFS is a file-server protocol. It doesn't enable interoperability," McInnis says. In contrast, NAS can link VMS or Ultrix work stations in a multivendor computer environment, enabling MS-DOS applications to run on DEC platforms and permitting file sharing with Apple Macintoshes.

Gaubatz stresses that the sheer number of VMS users—some 8 million—will also fuel DEC's growth in work stations. "If even a small fraction of those move to work stations, that means a solid base for us," he says. *–Lawrence Curran*

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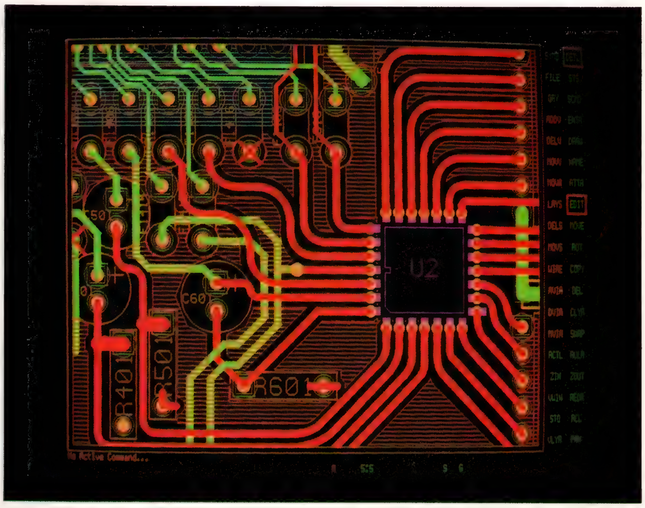

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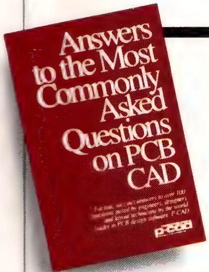

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Circle 300

Programmable
Logic Devices

NEW LIFE FOR

The boom in work stations is fueling growth for PLDs, while chip makers toy with architecture to boost speed and density

BY BERNARD C. COLE

The hot new high-volume logic market that has semiconductor houses rubbing their hands in anticipation is not so new at all. But process and circuit-design technologies that boost speed and density by an order of magnitude are transforming the venerable programmable logic device into a billion-dollar baby.

PLD market growth is being driven by the requirements of microprocessor-based systems, particularly work stations and personal computers. As these machines increase in speed from less than 10 to at least 40 MHz—and in word and bus size from 8 and 16 to 32 bits—they need circuits that operate faster and are denser, while using less power.

To get what they need, system designers are nixing small- and medium-scale-integration parts in favor of PLDs, says Andy Robin, director of programmable logic marketing at Advanced Micro Devices Inc. in Sunnyvale, Calif. In fact, says Dane Elliot, director of applications engineering at Cypress Semiconductor Corp. in San Jose, Calif., most high-performance work stations and PCs would not exist without PLDs.

Until relatively recently, the PLD market never exceeded a few hundred million dollars a year. Because of architectural, power, and speed limitations, PLDs served only a dozen or so limited niches. But thanks to the technology advances and the boom in work stations and PCs, worldwide PLD sales this year should double the 1987 totals to top $1 billion, says market watcher Dataquest Inc. of San Jose. By 1994, Dataquest says, PLDs should approach $1.8 billion in annual sales.

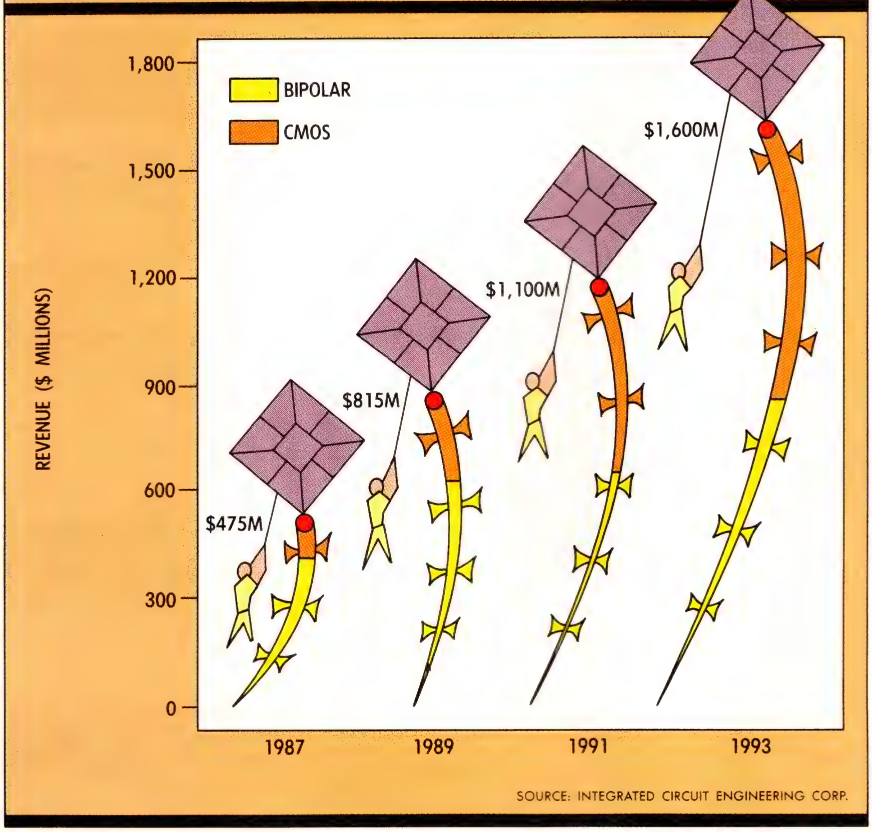
With this kind of market growth, it's no surprise that the number of PLD players is increasingly rapidly. At least 20 companies are now in the market; 16 of them are U. S.-based, two European, one Japanese, and one Korean. At least two other Japanese firms plan to enter the market in the next few months.

The boom comes none too soon for many U. S. semiconductor companies, faced with a declining market for standard logic on the one side and the emergence of mask-programmable gate arrays on the other. As they move to higher densities, PLDs offer U. S. companies a way of meeting the application-specific requirements of their customers with a family of generic devices that can be produced in high-volume, jelly-bean fashion and then customized by the user. This trend in PLD production counters the Japanese dominance in mask-programmable arrays, which they have turned into a commodity-like offering.

From their origins as a way to collect random glue logic in a system into a single device, PLDs are taking on a larger and larger role, replacing not only MSI and SSI-type glue logic but also VLSI peripheral logic functions. PLDs are being used in control functions for cache, random-access memory, local bus, interrupt, disks, and local-area networks, and as input/output interfaces, timer-counters, and clock generators.

The diverse requirements of this fast-growing application area are changing the complexion of the PLD market—most

UP, UP, AND AWAY FOR CMOS PLDs



SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

AN OLD PART

dramatically, in the move from bipolar to CMOS. Where in 1987, about 15% of all PLDs were CMOS-based, this year the figure will be 37% and in 1994, 63%. In the declining bipolar segment, TTL PLDs, long the workhorse technology, will have to share what is left of the high-speed portion of the market with the newly emerging emitter-coupled-logic PLDs. From a minuscule market share last year, the ECL segment is expected to double in sales each year. By 1994, Dataquest says, ECL will account for about a fifth of the $500 million bipolar market.

In the CMOS segment, CMOS-based erasable and electrically erasable PLDs will continue to grow rapidly, constituting at least half of the CMOS PLD business through the mid-1990s. These parts will represent some $800 million in sales in 1994, Dataquest says, against $300 million this year. Growing even faster is a whole new category of CMOS devices that offer unprecedented densities. Among them are programmable gate arrays and what Dataquest defines as programmable multilevel logic.

Where current PLD architectures reach about 1,000 or 2,000 gates, these new architectures boast at least 10,000 gates and may soon deliver 20,000 or even 40,000. At those densities, PLDs will compete with traditional arrays for at least 90% of the available market, says Ross Freeman, vice president of engineering at Xilinx Inc. of San Jose.

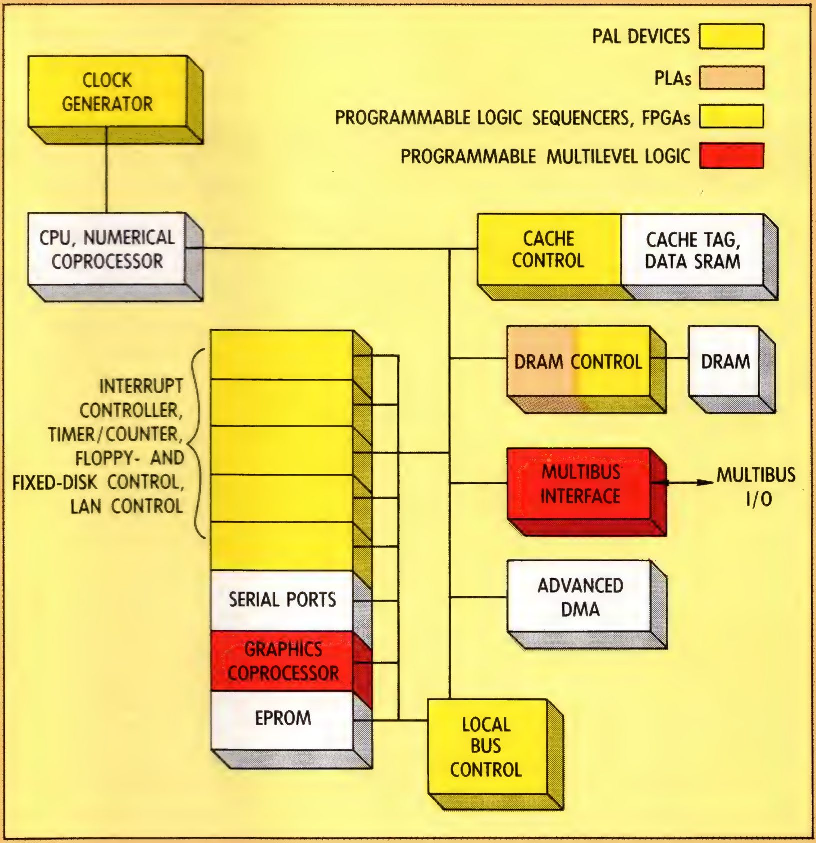
Moreover, they will change the way PLDs are used, says Terry Leeder, vice president of customer-specific products at Signetics Corp. of Sunnyvale, Calif. While the bulk of PLD sales will be to replace combinatorial glue logic, Lederer says, such usage will drop from the present 77% to 58% in 1992. Picking up the slack will be an increasing use of PLDs in timing and control functions (from 18% to 29%) and in system-level bus control and peripheral functions (from 5% to 13%).

Besides density, the other concern is speed. Using every bit of process expertise at their command, companies such as AMD, Cypress, Gazelle, National Semiconductor, Signetics, and Texas Instruments have pushed bipolar TTL PLDs from 20 or 25 ns down to 7 to 15 ns, and ECL PLDs to below 5 ns. On the bipolar side, the speed record goes to National Semiconductor Corp. of Santa Clara, Calif., which this month introduces a family of ECL PLDs specified at 2 ns using its second-generation Aspect bipolar process (see p. 74). In CMOS, Lattice Semiconductor Corp. of Beaverton, Ore., uses its Ultramos III process to get speeds in the 10-to-12-ns range. Other companies—including AMD, National, and SGS-Thomson—are pushing lithography below 1.0-μm to squeeze all the speed they can out of their CMOS processes.

An alternative to higher speed for CMOS PLDs is to use an architecture-specific approach, tuning a device's internal circuitry to the requirements of particular microprocessors. For example, Cypress this month is unveiling a proprietary state-machine EPLD targeted at the high-performance requirements of systems based on reduced-instruction-set-computing processors with the 125-MHz CY7C361 (see p. 74).

Similarly, looking to support its family of 32-bit 80960 embedded processors, Intel Corp. has just introduced the 6-ns 85C960 burst-mode CMOS PLD, which can run in systems with clock speeds as high as 25 MHz. The Santa Clara company's chip is organized as 16 dedicated inputs feeding a programmable decode array, with eight latched outputs controlled by a global clock. Key to the high performance is a novel pipelined architecture integrating an on-board latch function. Most present CMOS PLDs operating in

HOW PLDs ARE USED IN SYSTEMS



PLDs are omnipresent in high-performance work stations and PCs, where they are used for a host of timing and control functions.

the TTL environment use a TTL/CMOS level translator, then inverters and buffers to drive data through an array of programmable elements. In the Intel device, the on-board latch allows for loading data into shift registers and steering the inputs through the array, enabling it to be used in pipelined applications with multiplexed address and data buses.

Responding to the needs of designers of microprocessor-based systems, traditional PLD manufacturers such as Altera, Exar, Signetics, and others have been looking for ways to boost density without totally abandoning familiar and well-understood technologies. Among these are the programmable logic array with its programmable AND, programmable OR architecture and the programmable-array-logic setup, based on programmable AND, fixed OR.

The result of their tinkering is a new category of devices: programmable multilevel logic, with up to 6,000 equivalent gates. Included in this category are NAND/NOR-based arrays from Signetics and Exar that feed a signal back around a core array, to which is attached a variety of high-level logic functions. This way, devices can incorporate several levels of logic that with traditional PLDs would require separate parts.

Also in this category are more recent devices such as Altera Corp.'s EPROM-based mutliple-array matrix family and International CMOS Technology Inc.'s EEPROM-based PEELarrays [*Electronics*, March 1989, p. 86]. The latter consist of multiple small PLD-like structures linked by a programmable interconnect.

At the other extreme are a handful of companies that have thrown away the rule book, opting for field-programmable gate-array architectures that may one day push densities to the tens of thousands of gates. The pioneer in this category is Xilinx, which currently offers 3,000- and 9,000-gate static-RAM-based parts and has plans for a 20,000-gate device by the end of the year (see p. 76). Another player is Actel Corp. of Mountain View, Calif., with its one-time-programmable antifuse-based ACT1 CMOS gate arrays [*Electronics*, Feb. 18, 1988, p. 75].

The newest player is Plessey Semiconductor Ltd. of Swindon, UK, which this month unveils the first in a family of SRAM-based electrically reconfigurable arrays that start at 10,000 gates.

Plessey's initial device, the ERA60100, is built around an array of cell elements, each consisting of a simple two-input NAND gate and an associated 8-bit SRAM for programming interconnections. The architecture is extremely scalable, says Steve Brightfield, marketing manager of CMOS arrays. With present technology, he says, 40,000-gate parts are within easy reach. □

NATIONAL SETS A SPEED RECORD AT 2 NS

National Semiconductor Corp. has moved into the lead in the race to provide the speediest field-programmable logic devices. The Santa Clara, Calif., company this month started sampling 24- and 28-pin emitter-coupled-logic and TTL parts that break the 5-ns speed barrier.

The first of these are the 2-ns PAL1016 and PAL10016C4-2, both ECL input/output-compatible programmable-array-logic circuits with four output and 16 dedicated input functions. The parts, 10K- and 100K-compatible, respectively, are 30% to 50% faster than comparable parts now available.

A new transistor structure and Aspect II are the keys

In the works are TTL versions that, at 5 to 6 ns, compare favorably with current-generation ECL devices and with higher-density devices such as the 22V10 and the 13RL8, says Jay Kamdar, director of marketing for programmable logic.

There are two keys to the high performance and higher density, says Rick Walker, strategic marketing manager for programmable logic. Both come by way of a new tungsten vertical transistor structure combined with Aspect II, a 1.5-µm, 120-ps version of the contactless Aspect bipolar process that National acquired when it bought Fairchild Semiconductor Corp.

Walker explains that conventional fuse-link bipolar PLDs are based on a two-dimensional array of cells, in which each cell consists of a diode in series with an electrically conductive thin-film metal element. This scheme has drawbacks: since the fuse lies on the surface of the silicon, it takes up a significant amount of space. Also, Walker says, this lateral fuse approach does not lend itself well to full testing of the device's programming and electrical characteristics.

National uses an avalanche-induced-migration vertical fuse, which is essentially a simple transistor with a floating base, to overcome these limitations. The actual fusing takes place within the silicon at the emitter base junction; according to Walker, a controlled current is forced into the transistor's emitter, inducing avalanche breakdown of the emitter base junction. The cell is less than one-third the size of a conventional thin-film fuse-link cell.

While a few other companies, such as Signetics Corp. of Sunnyvale, Calif., have started using vertical fuse structures, the National implementation is unique because of Aspect. Since the process is contactless, there is no metal contact line. Rather, polysilicide runs above the base and collector regions, linking base and collector electrodes and eliminating the need to connect them with a common metal contact point.

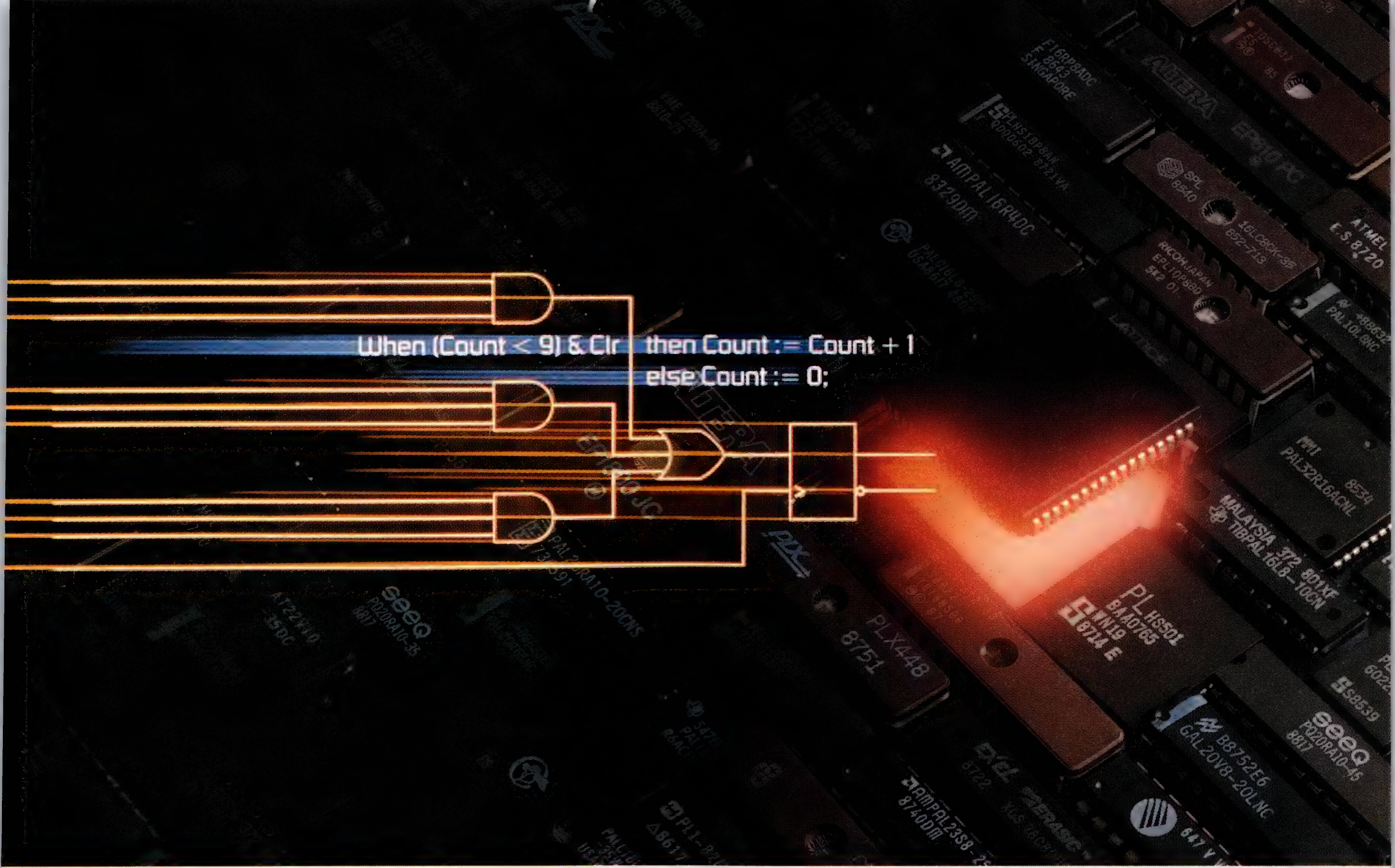
Because the polysilicide can be extended in any direction throughout the substrate, any number of transistors or logic elements having common points can be interconnected. And because the polysilicide can short two doped layers, fewer contact windows need to be opened on the chip, making more area available for active devices.

Kamdar says that by year's end National will begin sampling a family of 20-pin TTL PLDs rated at 5 to 7 ns. Also, he says, with a third-generation Aspect process now in the works, National will be able to build 20-, 24-, and 28-pin TTL PLDs that break the 5-ns barrier, as well as 1-ns ECL devices. *–B. C. C.*

KEEPING PACE WITH SYSTEM SPEED

Designers of personal computers and work stations today have a problem: conventional programmable logic devices cannot keep up with the new generation of high-performance microprocessors used in these machines. Now one chip maker says it has the answer to this designer's dilemma.

Because of system considerations and their internal architectures, PLDs must operate at twice the clock frequency of the central processing unit. Today's fastest bipolar or CMOS PLDs top out at 33 to 40 MHz, which means they're too slow for the new breed of processors running at 30 to 35 MHz and beyond. Although emitter-coupled-logic PLDs have



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enough speed to do the job, they are power-hungry, which defeats the purpose of using low-power CMOS logic in the rest of the system.

Cypress Semiconductor Corp. of San Jose, Calif., says it has devised a way to solve the speed problem without moving to an exotic technology such as ECL, biCMOS, or gallium arsenide.

The company's circuit designers have been able to boost internal clock rates to 125 MHz by incorporating a grabbag of imaginative circuit-design and architectural innovations.

These include the use of a split-plane architecture, an independent path for the latch-enable signal, a condition-decoding input logic structure, an on-chip clock doubler, and a signal-conditioning circuit, as well as reconfiguration of the register feedback network.

The 125-MHz Cypress parts are fast enough for today's CPUs

The first PLD to employ these techniques, the 28-pin CY7C361 programmable-state machine, achieves its 125-MHz clock rate with little or no boost in power consumption; it uses just 700 mW, one fourth to one fifth that used by ECL devices with comparable performance. The new device will be available in sample quantities later this year.

Al Graf, programmable logic marketing manager at Cypress, says the split-plane architecture and the use of the independent delay path for the latch-enable signal are the two most important contributors to the performance improvement. Unlike most other programmable chips, which have the state registers fed by the output plane, the CY7C361 has its 32 state-register macrocells situated between the input logic plane and the output OR plane to reduce and balance the propagation delays. This structure allows the circuit to operate with external clock frequencies of more than 66 MHz and internal frequencies of 125 MHz. The separate delay line for a latch-enable signal also reduces delay times.

The array architecture also features an unusual logic structure that employs a scheme called condition decoding, which combines AND and OR logic. This scheme helps minimize delays and makes the overall circuit more efficient, since signals do not encounter the delays they would in a programmable-array-logic device. □

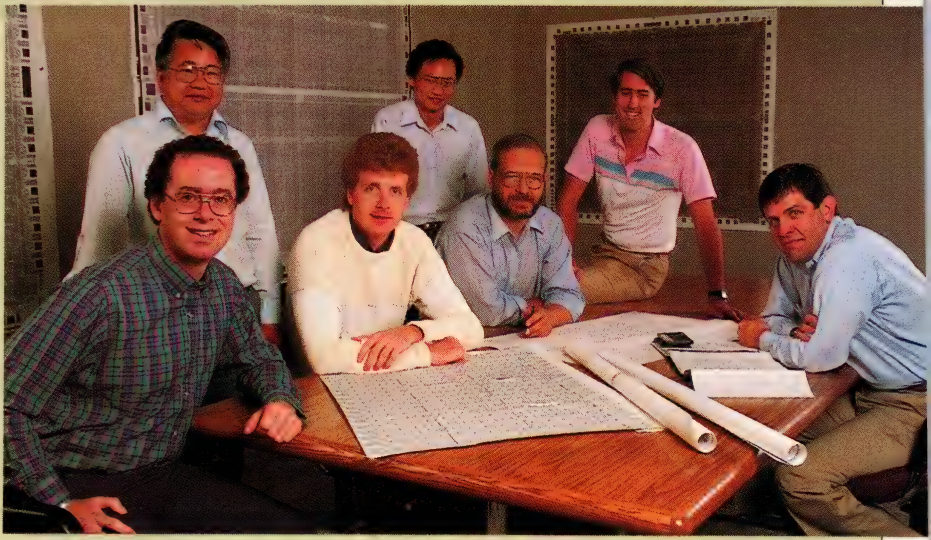
XILINX GETS GATES GALORE WITH AN SRAM SOLUTION

If imitation is the sincerest form of flattery, executives at Xilinx Inc. should be blushing with embarrassment.

A few years ago, the San Jose, Calif.-based company stood alone as a supplier of programmable gate arrays, with offerings based on static random-access memories rather than the more conventional electrically erasable programmable read-only-memory or EPROM technology typically used in programmable logic devices. Now that the competition is heating up, Xilinx is leveraging its experience to remain a leader in a fast-growing portion of this market.

Xilinx's ability to quickly meet user demands for increased gate density has translated into impressive financial performance. Since 1986, the company has racked up 12 straight quarters of steady growth. Revenues for the fiscal year ending in March 1989 topped the $30 million mark, more than double the previous year's performance.

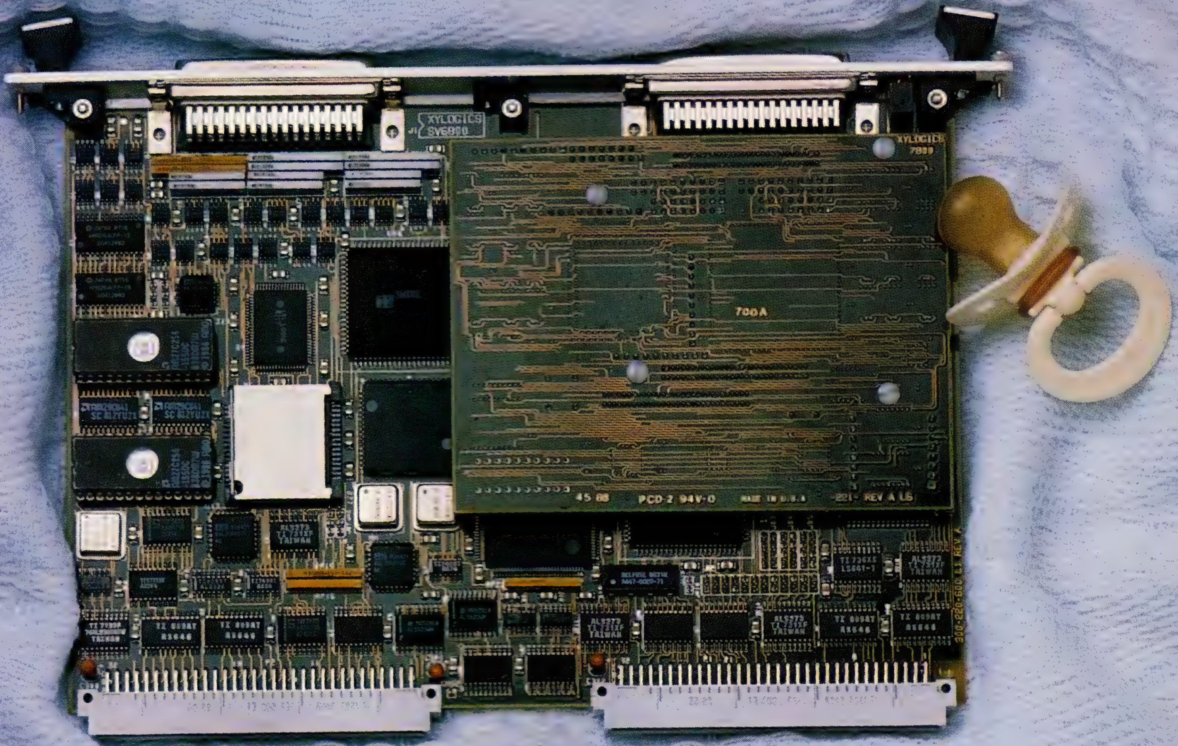
As recently as two years ago, most PLD manufacturers were still skeptical about SRAM-based field-programmable gate arrays, notes Ross Freeman, vice president of engineering and one of Xilinx's three founders. "Their argument was that the users would not go for an SRAM solution if there was a nonvolatile alternative available and that it would never reach more than a small portion of the total market," he says. Users, however, were more concerned with finding a proven technology with an upgrade path and were willing to forgo nonvolatility, according to Freeman. While PLD makers have stalled at about 2,000 gates in density, Xilinx's current XL3000 family offers 2,000 to 9,000 gates.


The 4000 design team, clockwise from left: Bill Carter, Steve Tremberger, Chuck Erickson, Jim Hsieh, Art Reynolds, Jason Ja, and Steve Perry.

More than 2,000 companies now use Xilinx's SRAM-based products; the company has also sold some 4,000 development systems. At present densities, says Freeman, Xilinx will account for about half the 24,000 gate-array designs that will be finished this year.

A number of companies are rushing to get into production with high-density field-programmable gate arrays or gate-array-like PLDs, pushing their processes and stretching their architectures to the limits to achieve densities ranging from 5,000 to 10,000 gates. Xilinx has not been standing still; Freeman says its new structured programmable gate array family, the XL4000 line, pushes densities to 20,000 gates and system clock rates up to 70 MHz, a 50% improvement over the XL3000 family.

With its new product line, which is slated to be in volume production by the beginning of next year, Xilinx will meet the requirements of more than 90% of the gate-array designs being done today, Freeman asserts. "We pioneered the field-programmable gate-array market," he says, "and we want to reap the rewards of that effort. We do not plan to make it easy for competitors to get in." *–B. C. C.*



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BY WESLEY R. IVERSEN

AUTOMAKERS SPREAD THE WORD: MORE ELECTRONICS

It's been more than a decade since the first VLSI engine controllers showed up in American-made cars. Auto engineers, being mechanically inclined, designed intelligent chips into their vehicles somewhat reluctantly at first. But they came to view the chips as a way to help meet then-emerging federal fuel economy and automotive emission requirements.

Few engineers in Detroit imagined at the time the extent to which embedded computers would one day catch hold in the family buggy. Nor did they foresee how much computing horsepower they eventually would need.

Coming by 2000: navigation, guidance, car-to-satellite communication

Today, microcontroller chips are not only proliferating in luxury cars to control an ever-growing list of new electronic automotive functions, but they are also working their way into volume applications in economy vehicles, for jobs like antilock brake systems and fuel injection. As North American automakers look down the road at their future computing needs, they are still sometimes surprised at what they see. Indeed, if even a fraction of the features that some now envision for the cars of the year 2000 and beyond get into production—features like navigation, collision avoidance and guidance systems, fully active suspensions, and direct car-to-satellite communication links—the requirements for integrated number-crunching power in automobiles could become enormous.

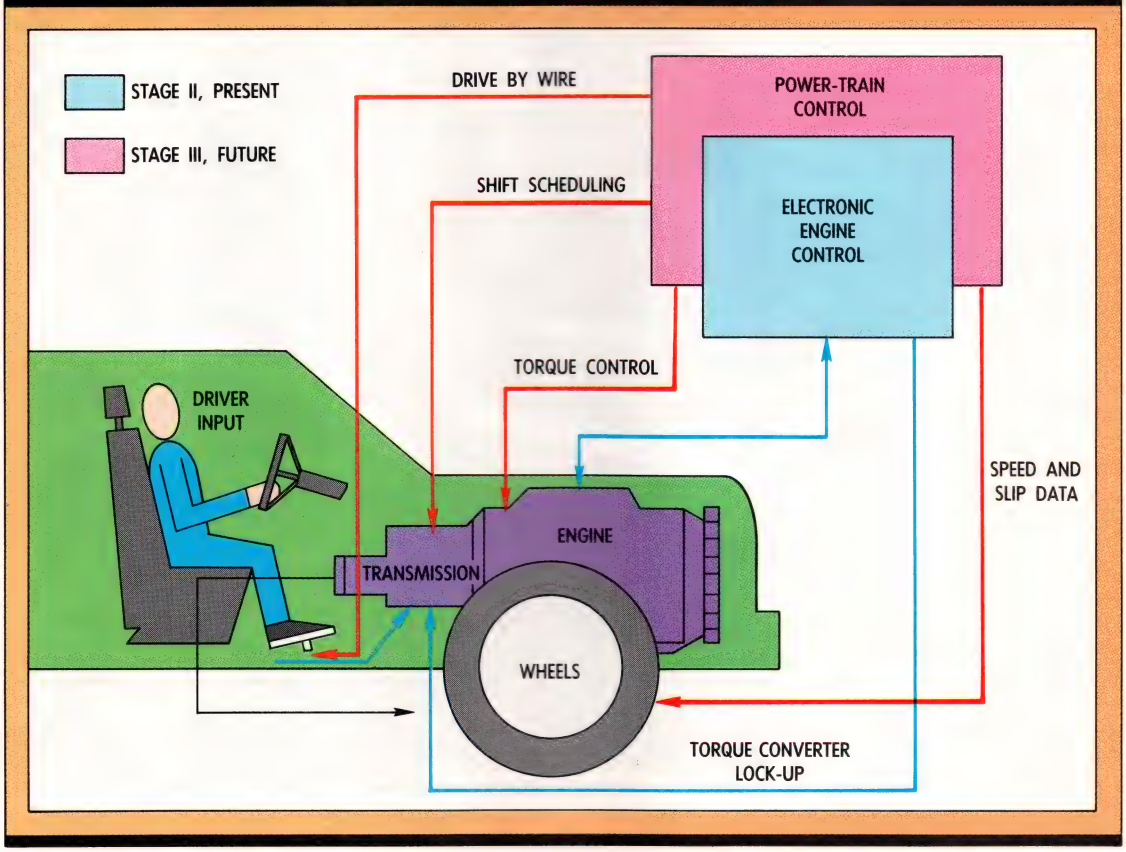
The typical U. S. car today carries two to three separate electronic control modules; that number will grow to five or six by the early 1990s, predicts Greg Shepperd, an analyst with market researcher Dataquest Inc. in San Jose, Calif. Some high-priced cars already are outfitted with 30 or more separate electronic modules. As soon as 1993, some observers predict, the average electronic content per vehicle will be worth $2,000, up from around $900 today.

The direction seems clear. By various estimates, the worldwide transportation semiconductor market will more than double to $4.7 billion between 1988 and 1995. Big gains are expected in several categories, including smart power chips, analog circuits, and sensors [*Electronics*, July 1989, p. 54].

One of the most vigorous segments of the market will be in single-chip computer circuits. Worldwide shipments of 4-, 8-, and 16-bit microcontroller chips accounted for about 15% of the total vehicle semiconductor market last year. Market watchers expect that figure to grow to $900 million, or nearly a fifth of the total, by the mid-1990s.

In North America, automotive is both the largest

MOVING TOWARD FULL CONTROL



In the second stage of auto electronics, automakers shifted from individual components to modules linking components. In the third stage, electric and electronic subsystems will be totally integrated.

and the fastest-growing segment of the embedded microcontroller marketplace, says Shepperd. He sees revenues from automotive chips doubling to $375 million between 1988 and 1994.

Eight-bit chips, which sell for $2 to $3 each in volume and make up about 65% of the North American automotive business today, will still hold sway by mid-decade. But 16-bit and larger machines will show the biggest revenue growth, according to Dataquest, jumping from $24 million last year to $110 million in 1994. The market for 4-bit controller chips, conversely, will fall off, dropping from $40 million to $30 million in the same period, the market researcher predicts.

In North America, more than in other parts of the world, the push is on to develop highly capable automotive chips. Already, U. S. automakers are planning a new generation of powerful engine controllers for rollout in the mid-1990s. And the trend here seems toward centralized vehicle architectures, as opposed to the distributed, multiplexed control schemes favored by the Europeans (see p. 82).

Most notable is General Motors Corp.'s plan to make the jump from an 8-bit all the way to a 32-bit auto chip architecture. The Detroit automaker says it will introduce production cars around mid-decade using controllers based on the 68332 chip, developed jointly by Motorola Inc. with GM's Delco electronics unit, based in Kokomo, Ind. Billing it as "the first 32-bit microcontroller ever," Motorola introduced the chip to the open market last April as the first in a family of machines to be aimed at a variety of automotive and nonautomotive applications.

For the 1994 model year, Ford Motor Co. of Dearborn, Mich., is also planning a new, more powerful generation of its EEC-IV electronic engine control module. The unit will feature not one, but two Intel 16-bit 8065 controller chips and will integrate engine control with transmission control. The chips will work in a coprocessing mode, linked by a dual-port, random-access memory, with one chip probably handling the engine, the other committed to transmission functions.

The carmakers aren't limiting themselves to conventional microcontroller architectures. They are also studying the use of digital signal processors for selected applications in cars.

DSPs are already showing up in high-end digital audio entertainment systems. And Dallas-based Texas Instruments Inc., for one, says it's working with automakers and subsystem suppliers worldwide on a diverse set of potential automotive jobs for its TMS320 family of DSP chips. These jobs range from active suspension, four-wheel steering, and integrated antilock brake and traction-control systems to "electronic mufflers" that would wipe out engine sound by generating audio waveforms in opposite phase.

Detroit's push toward more powerful chips is driven by converging factors. Even as electronic functions proliferate in the car, vehicle designs themselves are becoming more compact and aerodynamic. That means less space in which to cram in more electronic

A worker at Delco Electronics checks a row of computer-automated burn-in chambers, where electronic engine-control modules are tested.

boxes. As a result, the automakers are moving to integrate functions that were previously handled separately, putting them under the control of a single centralized computer or microcontroller.

"What we don't want to do is what we've historically done, where every time we would add a feature, we'd add a box," says Dennis Florence, executive engineer for current platform engineering at Chrysler Motors Corp. in Highland Park, Mich. "What is happening, and what I believe will continue to happen, is that there will be some lesser number of boxes than there are systems supported by electronics in the car."

EMISSION CONTROL. Regulatory pressures also affect the picture. The auto industry for the first time faces the prospect of comprehensive emission requirements in Europe, with the emergence of a united market beginning in 1992. And in the U. S., automakers are looking down the barrel of stricter enforcement of emissions standards under President Bush, not to mention a schedule of increasingly stringent corporate average fuel economy measures.

"This is going to hit us real hard starting in 1994," one Detroit executive observes. "The industry basically went to sleep during the Reagan administration. And now Bush is bringing it all back to bear on us." This executive believes the auto industry will meet the challenge. "I think we're going to be okay," he says. "But it is going to put a lot more burden on electronic engine control features."

For the major suppliers of embedded automotive controller chips, the implications are clear. The carmakers will not only require more microcontrollers, but they will also need chips with more power, more memory, and more and faster input/output, as well as linear, on-chip functions like analog-to-digital conversion and better diagnostics.

Increasing use of electrically erasable programmable read-only memory will also be a trend, including conventional as well as flash EEPROM, the automakers say. Detroit will be looking for more software and high-level-language support, as well as vendors that can meet the auto industry's tough requirements for reliability and low cost. Testability is also a growing concern, since today's electronics are handling more safety-related functions, and the failure of a single centralized controller chip could not only wipe out multiple systems but also lead to big liability problems.

As the big chip vendors go after the business, they are working on all these fronts. And increasingly, they are developing new configurations of existing 8- and 16-bit machines as a way to meet expanding automotive needs.

Intel Corp., for example, offers versions of its 8-bit 8051 and 16-bit 80C196 family that feature memory, I/O, and other functions tailored for specific jobs like antilock brake control or eight-cylinder fuel injection. These chips typically start as customer-specific parts, but end up being spun out for general sale as what Intel calls application-specific standard products, says Fred Phail, strategic marketing manager for the automotive division of the Santa Clara, Calif., firm.

National Semiconductor Corp. takes a similar approach with its families of 4-, 8-, and 16-bit machines, says Paul Standish, director of automotive marketing for the Santa Clara company. National's three-year-old 16-bit HPC chip is offered in four configurations, and the 8-bit COP 888 used in antilock braking systems and elsewhere is offered in at least a half dozen versions, he notes. Though National currently doesn't sell chips into any engine control sockets, the company is the largest control chip vendor in antilock brakes, Standish says.

At TI, the marketing attack is two-pronged. At the high end, the company now offers about 20 variations on its TMS320 family of DSP chips for potential automotive use, says Kun-Shan Lin, mar-

HOW THE MARKET SHAPES UP

	1985	1988	1991	1995	Compound annual growth rate (%)
$/ vehicle	406	580	825	1125	NA
Semiconductors ($ billions)	1.5	2.2	3.3	4.7	12
Microcontrollers ($ millions)	221	335	572	900	15
Microcontrollers (units millions)	36	57	100	165	16.4

SOURCES: B.S.MACKINTOSH, DATAQUEST, FROST & SULLIVAN, INTEL, WARDS AUTOMOTIVE

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NORTHWEST AIRLINES

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keting manager for the line. And while Lin concedes pricing on high-end 320 products is still steep, some lower-end versions of the part have now dropped below $5 each in volume.

TI is also making a push for the high-performance 8-bit market with the TMS370, developed originally with Delco for use in entertainment and climate-control applications. The part is highly configurable and easily testable, and is already available in 16 separate standard products, says Michael Polen, microcontroller marketing manager for TI's Semiconductor Group in Houston.

At industry leader Motorola, whose 8-bit 68HC11 is used in high-volume applications by Chrysler and GM, the focus is on the high ground. "We're currently big in 8-bit, but we're making a giant leap for mankind to 32-bit," says Bill Van Tine, strategic automotive manager for the firm's Semiconductor Sector in Phoenix. His reference, of course, is to the 68332 commissioned by Delco.

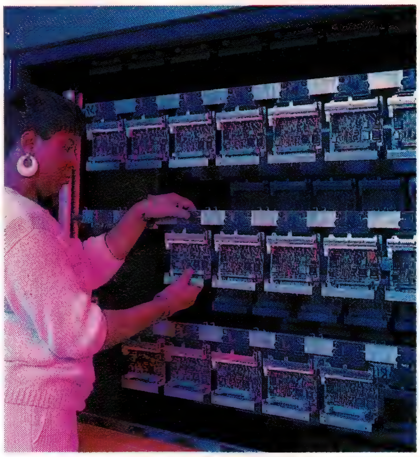
"In one sense, we skipped 16-bit because we believe that in the mid-1990s, the 32-bit machine is absolutely going to be required," Van Tine maintains. But Motorola is developing a 16-bit microcontroller, the 68HC16, he notes.

The 68332 relies on a 32-bit 68020 core with a 16-bit external data bus and features a modular design and configuration geared to autos. It can hit sustained performance rates of 10 million instructions per second, Motorola says.

On automotive engine control benchmarks run by Delco, 68332 throughput measured 10.7 times better than that of the 8-bit 68HC11. That's some 40% better than the throughput design goals in place when Delco started the project with Motorola in 1985, notes John Kastura, a Delco staff development engineer. GM's plans for the 68322 remain shrouded. But Kastura says the chips could show up in GM cars as soon as model year 1994 for use in complex power-train control jobs.

RAISING EYEBROWS. Despite its backers, the 68332 is raising eyebrows among some industry watchers. "I don't think there will ever be a need for it," declares Myles Kitchen, at M. H. Kitchen & Associates, a Santa Clara-based automotive electronics consultant. "GM will find a way to use it. But it's a case of creeping elegance. They've carried these products much further than anyone would have imagined four or five years ago."

Ralph V. Wilhelm Jr., Delco's director of advanced engineering and systems integration, sees it differently. In fact, he indicates, the opposite may be true. "I know that when the 68332 was being designed, there was the feeling that it was one hell of a machine, and that we would probably never see anything that would go beyond it," he says. "Now, I'm not so sure that's necessarily true any more, as powerful as it is. Looking back a few years, I don't think we could see far enough ahead to where the world was going, and what kind of capacity and throughput we'd really need for that machine." According to Wilhelm, Delco is already looking at one experimental system for use in a mid-to-late-1990s vehicle that requires not one, but two 68332 chips to perform needed functions.



Engine-control modules get a protective silicon coating.

While GM has made the move to 32-bit architectures, both Chrysler and Ford so far are hanging back. "Just because somebody else comes out with a 32-bit machine doesn't necessarily mean that we would," says Chrysler's Florence. And for the near term, he doesn't see the need to make the jump. Forthcoming emission requirements, coupled with other demands, could put Chrysler's current 68HC11 engine control system "on the hairy edge of its capability," Florence concedes. "But we're hoping that the basic [68HC11] machine or some variant of it can get us through the mid-1990s."

The story is similar at Ford. Given current trends, it has become apparent that the company's EEC-IV engine controller was running out of gas. But instead of investing money in a new chip design, Ford plans to extend the six-year-old EEC-IV architecture one more time, this time by adding a second 16-bit Intel chip. Moving to a coprocessor design in the same module reduces the cost to about one-third what it would be to do two single-chip EEC-IV modules, says John A. Sullivan, Ford's manager of advanced power-train electronics. And because of overhead reduction, he says, the performance of the dual-chip unit approaches three times that of the current EEC-IV.

Sullivan calls the two-chip EEC-IV "an interim solution," before a next-generation 32-bit machine that could meet Ford's needs by the late 1990s. The company is defining requirements for the next-generation chip, he says. Ford plans to select a vendor and kick off the design project next year. □

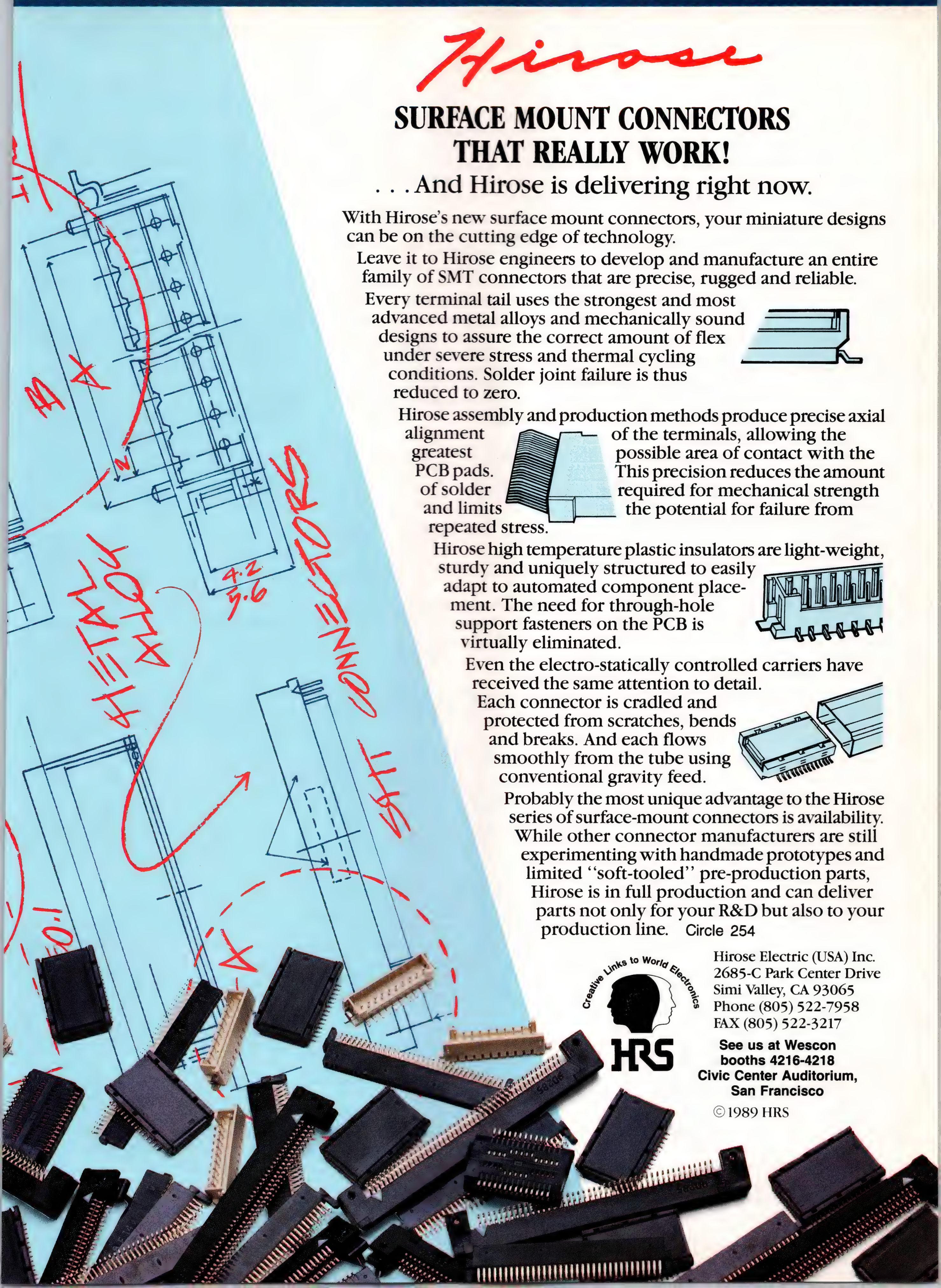
EUROPE GETS UP TO SPEED

By and large, Western European carmakers are following the same trends in microcontroller technology and applications as their U. S. counterparts. And although Europe lags the U. S. in market volume, with fewer controllers per vehicle, the Continent is catching up. At Europe's big three chip makers—Philips of the Netherlands, the Italian-French semiconductor combine SGS-Thomson Microelectronics, and West Germany's Siemens—experts predict that the European automotive microcontroller market will grow faster during the next few years than the U. S. market.

At present, European cars use only half as many integrated circuits, including microcontrollers, as do American-made vehicles, says Jürgen Lange, a director in Siemens AG's Semiconductor Division in Munich. One reason is that low-pollution exhaust regulations in many countries, particularly in Southern Europe, either don't exist or are less stringent than in the U. S. Also, for the small cars typical for Europe, complex electronic systems would account for too big a share of the car's cost.

As a result, although Western Europe produced more cars and trucks than the U. S. did last year—14.4 million units vs. 11.6 million—its automotive microcontroller market was much smaller, amounting to about $70 million in 1988, Lange says. This figure compares with the $187 million that the San Jose, Calif., market researcher Dataquest Inc. gives for North America that year.

But the situation is changing. As the 12 countries of the Economic Community, which are working to have common standards by the end of 1992, adopt stiffer antipollution legislation, more electronic controls in automobiles will be needed. And that trend, Lange points out, will



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help push microcontroller sales to $185 million in 1993, nearly three times their present level.

Forecasts from Philips International NV are even more bullish. Western Europe's automotive microcontroller market will be $500 million in 1994, says Dion Metzemaekers, manager of product marketing of MOS microprocessors at the company's Components Division in Eindhoven. The surge, he says, will come from more controllers going into small cars and from increased acceptance in Southern Europe.

As for technical trends, standard microcontrollers with ever greater complexity and number-crunching power are being widely applied to handle more than one function in a car. This trend is now accompanied by a move toward customer-specific modular controllers.

Illustrating the increasing use of more powerful parts are 8-bit controllers from European chip makers. Following the standard devices that have been designed into cars since the early 1980s, such as the 8051, are more complex 8-bit units that can handle, for example, fuel injection and ignition.

Typical is Siemens' 80515, a standard controller that hit the market in the mid-1980s and targets engine-management applications. It has since been upgraded to the 80C517, a controller with more powerful peripherals to meet the greater demands that engine management imposes on electronic control devices. Now, for applications in the early 1990s, the company is developing the cells for an 8-bit modular controller that will use dedicated peripherals.

8-BIT DOMINANCE. Eight-bit devices clearly dominate Europe's automotive microcontroller world. They will continue to do so well into the 1990s and, in terms of numbers, probably until the year 2000, predicts Alfred Hauenstein, marketing manager for automotive ICs at Siemens. At present their share is a whopping 90% of the total, with the remaining 10% accounted for by 16-bit and, to a small extent, 4-bit controllers.

With 8-bit controllers continually being upgraded in clock frequency, CPU power, and performance of on-chip peripherals, they are still far from the end of their useful life, Hauenstein says. "Most control needs in a car can be met with 8-bit devices until beyond the mid-1990s."

But the trend to more powerful 16-bit microcontrollers is under way. "While 8-bit devices continue to be adequate for most car applications, there's a move on to 16-bit microcontrollers for high-speed, high-end applications in engine management, and subsystem control," says Paolo Rosini, director of research and development in SGS-Thomson's VLSI Division in Agrate Brianza, Italy. But Rosini sees no immediate need for 32-bit controllers in cars. "They'll come at some future time for very high-end applications in complex adaptive control and automotive expert systems," he says.

All of Europe's major chip makers are on the 16-bit bandwagon. SGS-Thomson has brought to market its 8/16-bit ST9 series of devices, which are basically 16-bit controllers with 8-bit internal processing. These devices fit the current generation of antilock brake systems and handle engine-management functions. The company is also offering a 16-bit Transputer version from Inmos Ltd., the Bristol, UK-based firm that SGS-Thomson bought earlier this year. A general-purpose device, this Transputer version can be customized for specific control functions in the car, Rosini says.

Though Europe trails the U. S. in market volume, with fewer controllers per car, the Continent is catching up

Siemens, too, is ready for the 16-bit era. It is now winding up development of its 16-bit 80C166 controller, which it will start sampling toward the end of this year. The device is aimed at handling high-end engine management as well as antilock brake and traction-control functions.

For its part, Philips has the first implementations of 16-bit controllers—the company's 90C100 and 90C110, based on a 68000 core from Motorola—for use in cars. After a modest start, applications of 16-bit controllers in Europe will eventually outpace those of 8-bit devices, according to executives at both Siemens and Philips.

So with 16-bit controllers available, makers of car accessories are beginning to build these devices into their equipment. Stuttgart-based Robert Bosch GmbH, Europe's leading producer of engine-management systems, is introducing its sequential-injection Motronic M3 system for high-performance engines with six and eight cylinders.

In this system, the controller handles the flood of data fed to it via an 88-pin connector. The Motronic M3 automatically adapts itself to changing engine parameters.

As for centralized vs. multiplexed distributed controllers, Siemens's Lange sees more decentralized intelligence in store for cars "rather than a mammoth controller for handling everything." Metzemaekers of Philips agrees. "A distributed approach provides more flexibility and allows tackling isolated subsystems like antilock brake and car display systems for best economy, reliability, and efficiency," he says.

MAKING SENSE. Lange thinks a single controller has its place in the car to handle a number of functions. But these functions should be related—as are ignition, injection, and certain parts of the transmission system—and combined only if that makes sense, he says. Bringing together, say, engine management and electronic seat positioning doesn't make sense, he asserts. Another objection to a master controller in the car is that failure of such a device could spell disaster for passengers and the vehicle.

European semiconductor makers are divided over the issue of high-speed digital signal-processing chips for cars. Siemens experts say that since 16-bit controllers can handle high-speed processing, using DSPs would amount to engineering overkill.

But Philips's experts take an opposite view. They think that DSPs have a future in automotive applications to provide, for example, high-speed real-time control of suspension and navigation systems. But it won't be for another decade or so that DSPs will play a major role in cars. As the first step toward the DSP future, Philips is now working on a fast calculation unit giving a throughput comparable to that of a DSP and intended as a coprocessor for a microcontroller.

SGS-Thomson's Rosini says there's some interest from automakers in DSPs as an alternative to 16- and 32-bit microcontrollers and for applications in signal filtering and for specific engine- management tasks. For such jobs, SGS-Thomson has presented its ST18 family of devices to several customers. "But a market has not developed so far," Rosini says.

Philips has joined the group of companies backing the CAN multiplexing standard. In fact, its Components Division has been sampling a CAN controller in Europe and the U. S. since May this year—for about $5 apiece. The PCF 82C200 controls the CAN protocol and translates the signals on the bus to logic levels for use by microcontrollers. Product marketing manager Metzemaekers expects the controller to enter volume production next year and to be used in cars by 1991. *–John Gosch*

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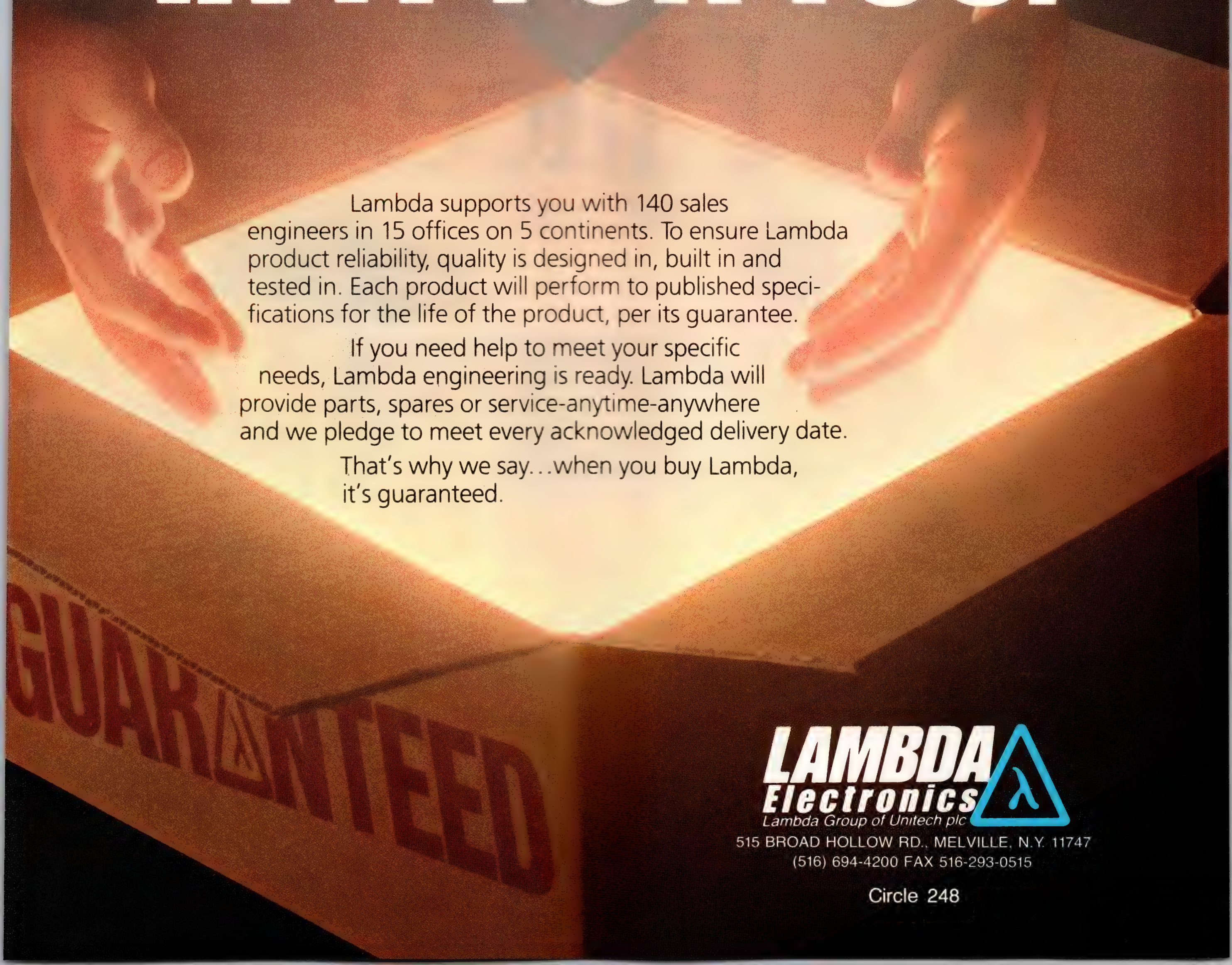

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BY JACK SHANDLE

Video conferencing breaks into the open

STANDARDS AND MODULAR ARCHITECTURES MEAN NEW OEM OPPORTUNITIES

After spending two decades in the wings, video teleconferencing is getting ready to rush onto center stage. Propelling this move are a soon-to-be-ratified international standard, a new breed of modular, inexpensive, open-architecture codecs, and tumbling telephone tariffs.

Because these changes are bringing down the price of video conferencing, new marketing strategies are being forged. Instead of selling at the corporate level, video-conferencing companies will focus on department managers with specific communications needs, says John Walsh, executive vice president of Compression Labs Inc., a leading video codec company based in San Jose, Calif.

For electronics equipment manufacturers, software houses, and systems integrators, this rising technology star can guide the way to new markets. Video conferencing will soon be inexpensive enough to be considered a normal extension of the telephone and flexible enough to be plugged into a local-area network. A wide-open field awaits companies providing windowing software, high-resolution scanners and monitors, multimedia technologies, and communications gear that allows screen-to-screen transfers without computer intervention.

Even chip makers can get into the act. So far, SGS-Thomson Microelectronics and its recently acquired Inmos Ltd. subsidiary have launched VLSI devices that implement the dis-

Video conferencing can take place in elaborately equipped rooms, such as this one, that simulate across-the-table meetings. Or it can move from site to site using modular gear.

crete-cosine-transform algorithm that is used in standards-based image compression. Other semiconductor vendors are ready to jump on that bandwagon, and more opportunities exist for specialized echo-cancellation chips and application-specific digital signal processors.

The market for video-conferencing equipment will grow at a compound annual rate of 33.4% between 1988 and 1992, according to Dataquest Inc., a market research firm in San Jose. Its fastest-growing segment will be at transmission speeds in the 384-Kbit/s to 2.048-Mbit/s range, where 46% growth is forecast. The total market in 1992 is expected to hit $140.9 million, Dataquest says, up from $31.6 million in 1987. Pricing will play a key role in the growth. The average end-user price of a codec was $65,500 in 1987 and is forecast to be $23,200 in 1992.

The major technology hurdle to the acceptance of video conferencing—incompatibility of the codecs built by various manufacturers—will fall by the wayside next year when the International Telephone and Telegraph Consultative Committee ratifies its H.261 document. H.261 will define the standard for the video-compression/decompression algorithm that will be used at 64-Kbit/s multiples of transmission speeds from 64 Kbits/s to 2.048 Mbits/s. Interoperability testing began under the auspices of Bellcore Corp. and Bell Labs last month. The first round of tests includes offerings from Compression Labs, PictureTel, and VideoTelecom.

"The idea is to prove out the algorithm and the standard recommendations to ensure there is enough detail so that different codec makers can come up with products that interoperate," says David Hein, president of VideoTelecom Corp. in Austin, Texas. The CCITT standard describes a discrete-cosine-transform algorithm that has been modified for motion compensation. Interframe prediction is the means of attaining motion compensation, says Hein.

Beyond the standards arena, makers of codecs—which are the heart of any video-conferencing product—are abandoning the restrictions of proprietary boxes for modular, open-architecture systems. For example, VideoTelecom's $35,000 Conference System 350 incorporates a PC AT bus for control functions. A standard Ethernet card can be used to plug the codec into a LAN, says Hein.

THIRD PARTIES SOUGHT. "For example, the Air Force wants to interface with Ethernet LANs and have live Lotus spreadsheets on the screen," Hein says. Using the PC AT bus means other cards can be plugged in as well, such as an IBM 3270 terminal-emulation card or an internal modem card. "We're very interested in third-party involvement," he says.

TRANSMISSION COSTS NOSEDIVE

Coast-to-coast pricing ($/hr)		
Switched 56 Kbits/s	**1988**	**1989**
AT&T	$ 45	$ 18
MCI	NA	$ 8
US Sprint	NA	$ 7
T1 (1.544 Mbits/s)		
AT&T	$614	$473
MCI	$538	$414
US Sprint	$530	$409

SOURCE: *ELECTRONICS*

Just as committed to modularity is Compression Labs, the current codec market leader with 60% of existing installations worldwide. The first models of the company's Rembrandt II series will be introduced Oct. 16. One model—the Rembrandt II/06—will operate at six multiples of 64 Kbits/s, from 64 to 384 Kbits/s. Its new architecture allows the series to be upgraded and modified and its board systems depopulated so that it can be tailored to a customer's needs.

Compression Labs' approach to modularity does not include an open-architecture bus such as the AT bus, but slots are available in the codec for third-party support, says Dave Belove, corporate communications director. The company is already working with third-party board vendors on high-resolution graphics functionality and will release specifications of its control bus to other vendors with bright ideas, he says.

Rembrandt II will use a discrete-cosine-transform chip as a primary means of reducing costs. "It replaces three printed-circuit boards for us," says John Walsh, executive vice president. The flexible architecture also features a multimode codec. This enables it to communicate with pre-CCITT-standard algorithms and makes for enhanced performance that goes beyond the common denominator of international standards. Every codec maker has tweaked its algorithm to deliver some value-added feature, and this will continue to be a selling point in the competition among manufacturers.

"Modularity also keeps costs in line for the user, because each location will have different needs," says Walsh. "While the corporate headquarters may need the capability of talking to virtually any codec anywhere in the world, a local office might need just one algorithm."

Another major contender, PictureTel Inc. of Peabody, Mass., is not as interested in open architectures, says Rob Mitro, vice president of marketing. PictureTel will keep its software-based architecture for another generation; since it is software-based, however, it is modular and easily upgradable.

Like Compression Labs, PictureTel will implement the H.261 standard in 64-Kbit/s increments, although its offerings will go up to 2.048 Mbits/s. Other major players in the codec market include Concept Communications of Dallas, which has an AT-based architecture; NEC America of Mountain View, Calif.; and GPT Video Systems of Stamford, Conn.

BIRD'S-EYE VIEW. Although video-conferencing technology has grown quickly, it is not without its gaps and bottlenecks. From a bird's-eye view, the goal in video conferencing is to simulate an environment in which both parties feel as if they are in the same room, says Doug Wilkens, marketing manager for Pierce-Phelps Corp.'s Audio-Video Systems Division. As a leading systems integrator of video-conferencing rooms, Philadelphia-based Pierce-Phelps counts among its clients such corporate giants as Sears, Roebuck and Co., along with several aerospace companies.

In corporate settings, Wilkens says, the conferencing technology must be transparent to the user. "Corporate executives are operating the room—not video or audio engineers," he says. Therefore, "operationally, the conference has to be the same as a normal business meeting. And that requires almost intuitive use of the technology."

Presenting graphical information is a major hurdle in teleconferencing. High-end graphics applications are in particular need of a technology fix, says Victor Reed, vice president of engineering at Keiper Associates Inc., a Fairfax, Va.-based video-conferencing hardware consultant. Reed would like to see a high-resolution scanner than handles multiple-size documents yet is easy to use. "Flatbed scanners with high resolution are

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Circle 280

being used now," he says, "but they are awkward in a conference situation." Overhead cameras offer a simple-to-use alternative, Reed notes, but their resolution—just 100 dots per inch—is "nowhere near the 400 dpi that some people want."

Transmitting computer graphics is another application area that needs the right product. "We need a mode to communicate over a digital communications link without a computer at both ends," says Reed. "I want to do it screen to screen."

Also, high-resolution monitors haven't attained the picture size needed in a conference environment, and there is no large-screen alternative on the horizon. The performance standard, says Reed, is the ability to read a standard, typewritten document at 10 feet. Large-screen projection systems are available, but they do not offer enough contrast to meet the brightness-contrast-resolution performance standard, he says. Reed adds that the conference room cannot be darkened like an auditorium to make up for the contrast deficiency.

Besides the display's physical aspects, video conferencing must deliver more functionality. "Our customers have been asking for windowing products," says VideoTelecom's Hein. "We expect to source them from a third party."

Audio communication—an often overlooked aspect of video conferencing—can stand some price-performance improvement too, says Timothy W. Cape, a principal at Cape Dixson Associates Inc., an Atlanta-based technology consultant. Here, the object is interactivity. Early half-duplex systems shut off the party that was not speaking, a tactic that's not conducive to interactivity or to simulating a real conference-room environment. So these systems have given way to sophisticated—and expensive—echo-cancellation schemes that can model changes in the room and compensate for them. "The echo-canceler units available today range from $6,000 to $10,000 just for the components," says Cape, "and there's a fit-up cost on the room as well."

HIGH-END GRAPHICS DESPERATELY NEED A TECHNOLOGY FIX, SAY CODEC VENDORS

Multimedia products are just beginning to make a dent in video conferencing. These audiovisual technologies are often controlled from a personal computer activated by touch screen. Using preprogrammed menus, an executive can move from one segment of a presentation to another simply by touching the screen. A whole new multimedia technology called presentation graphics is just now emerging [*Electronics,* July 1989, p. 72], and video-conferencing specialists are eager to use it.

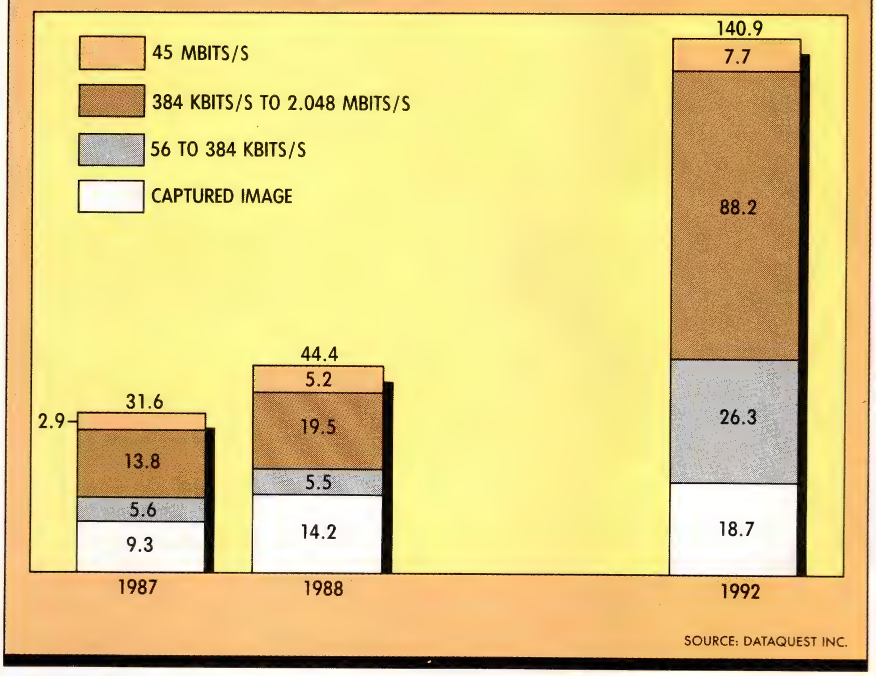
"If you can get multimedia integrated into a modular system," says Walsh of Compression Labs, "you have a market opportunity." At the high end, Walsh is particularly bullish on high-resolution graphics equipment in aerospace and government installations. "They need 1,000-by-1,000-pixel resolution," he says. "Since these people are involved in long-term, very high-cost projects, being able to reduce their project cycle time can mean great savings for them."

COST PLUMMETS. Hand-in-hand with the other market factors propelling video conferencing to a more prominent role in corporate communications is a precipitous drop in the cost of high-speed leased and switched telephone services. Over the past year, for example, AT&T Co. dropped its coast-to-coast, switched, 56-Kbit/s tariff by a factor of 2.5—down to $18 per hour. Competitors US Sprint Communications Co. and MCI Communications Corp. offer hourly rates of $7 and $8, respectively. For 1.544-Mbit/s leased lines, AT&T has dropped its price from $614 to $493 per hour over the past year, and its competitors have reduced their tariffs as well.

At the same time that transmission tariffs are dropping, the picture quality once available on expensive, high-bit-rate lines can now be acquired on lower-bit-rate lines, says Todd Clayton, VideoTelecom's marketing vice president. "Two years ago, you would have to lease a 768-Kbit/s line; now you can lease a 384-Kbit/s line and get the same picture quality," he says. "On top of that, the long-distance carriers are offering fractional T1 services. That's not very widespread today, but it will be soon."

With prices tumbling in both the equipment and network-charges sectors, video conferencing is getting closer and closer to being an extension of the telephone—and almost as ubiquitous. One salient example of a company committed to conferencing is Apple Computer Inc. The PC manufacturer has already installed a video network that puts video on the desktop in its Cupertino, Calif., headquarters. With the proper add-in cards and the addition of a few codecs, employees can have desktop conversations with remote sites as far away as France or Asia. ☐

READY FOR TAKEOFF



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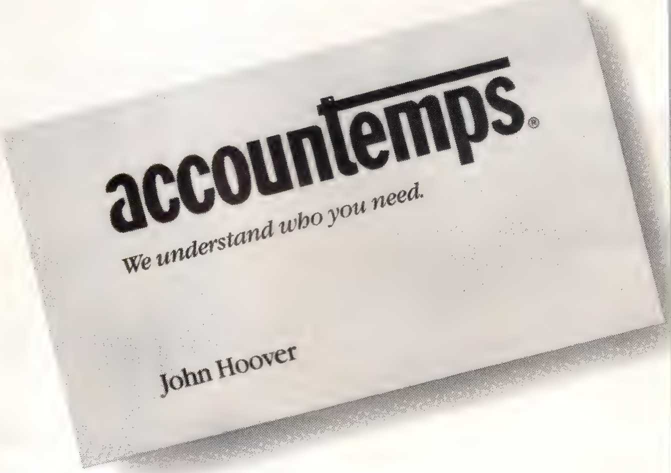

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Technology Outlook:
MOVING BEYOND HARDWARE

TI's push in the '90s includes semiconductor savvy, systems integration, and software—not necessarily in that order

BY SAMUEL WEBER AND BERNARD C. COLE

With markets undulating and technology constantly on the move, how will the big semiconductor houses negotiate the 1990s? If Texas Instruments Inc. is any indication, they will start edging into systems integration while simultaneously maintaining their commitments to next-generation chip technology.

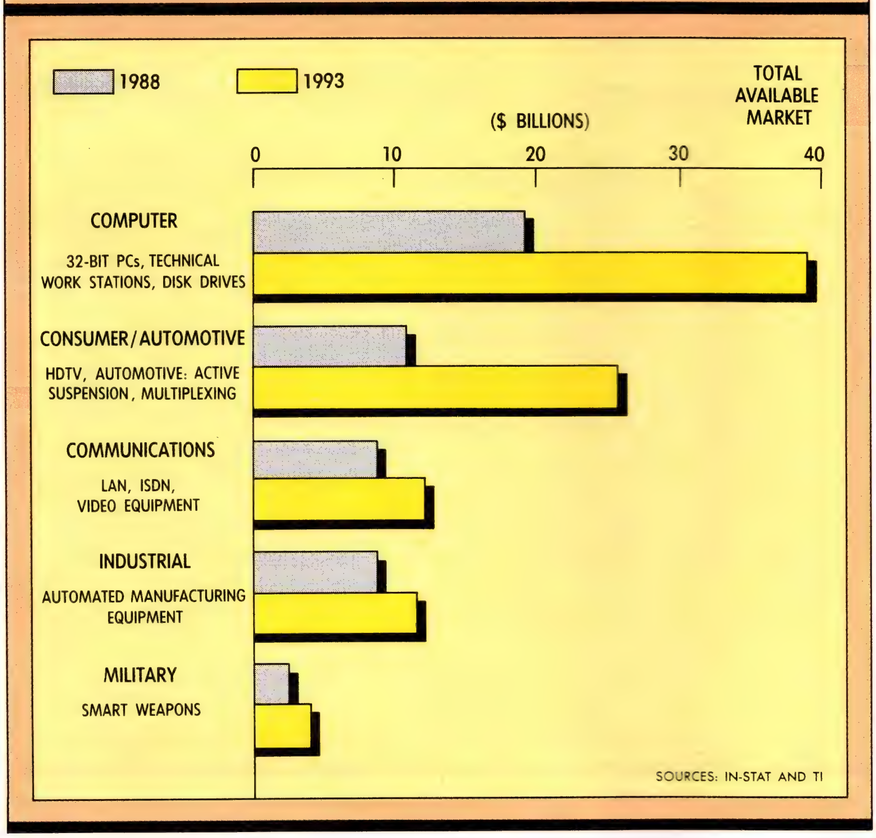
At the core of TI's strategy for the next 10 years is the application of its chip savvy in high-volume markets—not only in computers, but also in the consumer, auto electronics, and telecommunications sectors. But as the electronics industry moves toward the trillion-dollar mark in the 1990s, the giant semiconductor company is also targeting areas arising from the information-management revolution now under way. To exploit those opportunities, TI for the first time is offering the outside world products developed for its own management and manufacturing operations over the last five decades.

This was the technology outlook TI described for analysts and journalists at its annual product and market forecast last month. While the Dallas company in the past has confined itself to projecting one or two years out, this year it unveiled strategies, goals, and expectations for an entire decade—through the year 2000. What TI does may or may not be typical of the course the rest of the chip industry will take. But the broad-ranging plans suggest one direction the industry may follow as it ponders its future on the cusp of the 1990s.

Leveraging the know-how accumulated by its Defense Systems and Electronics and Data Systems Groups, TI is moving aggressively into what could be interpreted as a systems-integration role. And in this aspect of its business, the company is shifting emphasis from hardware to software.

"The challenge of the 1990s will be to extract information from data to provide real-time solutions for customers," says says William P. (Pat) Weber, ex-

WORLD SEMICONDUCTOR MARKET



SOURCES: IN-STAT AND TI

ecutive vice president. In TI's view, the idea of computing is shifting from a data-processing, number-crunching discipline, where speed is the essential measure of effectiveness, to an information-processing operation, where breadth of coverage determines performance. In other words, raw computing speed is less important than issues such as the amount of information available, the ease with which it can be accessed, and the forms in which it is available.

This change opens up opportunities for TI in areas outside its traditional semiconductor, defense, and digital systems operations. The company can bring to bear an arsenal of skills and emerging technologies that include networking, object-oriented programming, data-base management, multimedia user interfaces, artificial intelligence, and computer-aided software engineering. And at the core of the strategy is an adherence to open standards, using Unix and work stations designed around Sun Microsystems Inc.'s Sparc microprocessor.

In semiconductors, TI expects to build on its success in developing specialized microprocessors for graphics, local-area networking, and digital signal processing, Weber says. It plans to move in a big way into the reduced-instruction-set-computer market, using Sparc as the linchpin.

One intensive area of effort, says Weber, will be in consumer electronics, which he says constitutes almost half of the Asia-Pacific semiconductor market. Building on its expertise in application-specific integrated circuits and linear and memory technology, TI is making continued inroads into the Japanese market. For example, Weber says, Sony Corp. is now a major customer of TI in Japan and has decided to continue the relationship worldwide, with about 50 projects in joint development. In addition, says Weber, TI's linear and ASIC devices are being designed into the motor drive of Hitachi Ltd.'s video cassette recorder. "With this product in the heart of a Japanese VCR system," he says, "we have gained initial entry into a market once thought impenetrable to foreigners."

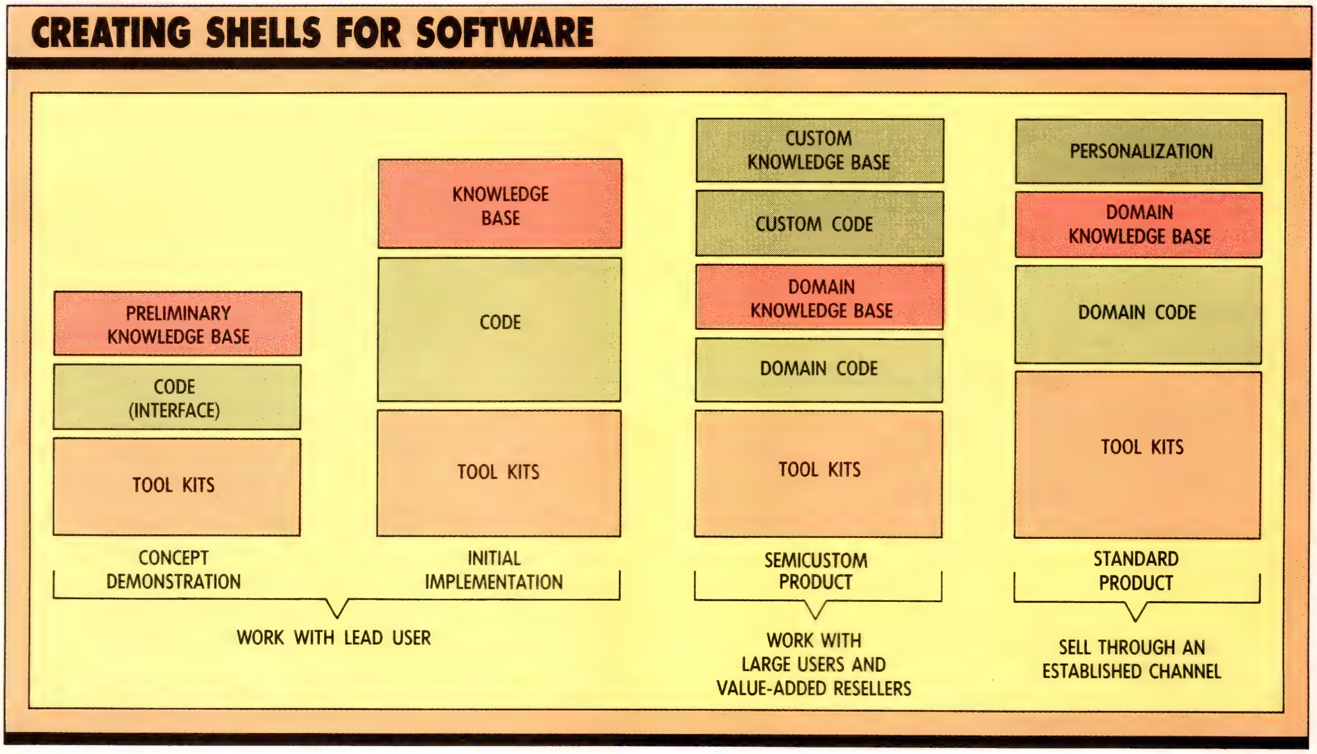
Raw computing speed is less important than issues like the amount of information available, the ease with which it can be accessed, and the forms in which it is available

In automotive, says Weber, TI is looking to increase its electronic content three- to fourfold. Its 8-bit reconfigurable microcontroller has met with considerable success already. With it, more than 30 custom applications are in development with such U. S. manufacturers as Delco, General Motors Corp.'s electronics unit. These jobs range from audio controls to air conditioning, heating controls, and antiskid braking.

In telecommunications, he says, major joint development products are under way worldwide, including one with a big European customer to develop a broadband switching system. The system will serve as a basis for high-speed communications setups supporting voice, data, image, and high-definition TV signals.

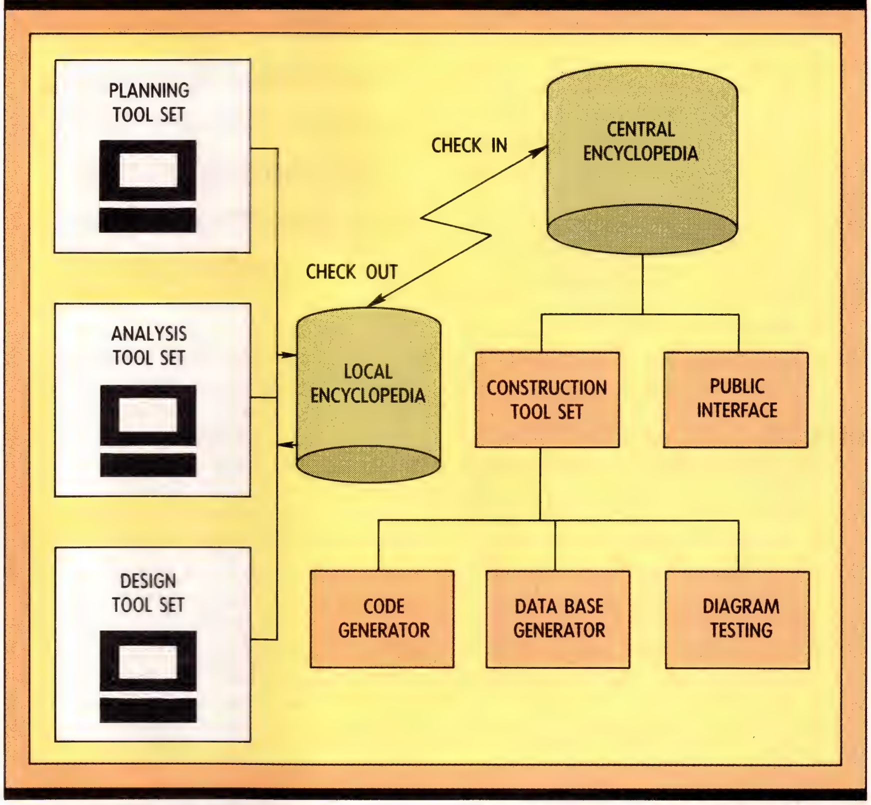
Cutting across all these efforts, says Weber, will be a continued focus on memory, particularly dynamic random-access memories. "One of the dramatic changes we will see in the '90s will be a significant increase in memory use in noncomputer applications," he says. "Not only are new generations of computers using several times the memory of previous generations, but the memory content of such products as fax machines, copiers, and laser printers is exploding. By the mid-'90s, noncomputer applications will constitute almost 40% of the memory market."

Besides specific custom and standard products in these application areas, TI has evolved an increasingly semistandard, user-specific logic and memory strategy. In the VLSI building-block area, TI has shifted from a standard building-block approach based on bit-slice, general-purpose processors and coprocessors to one based on application-specific and customizable processors says Wally Rhines, executive vice president of TI's Semiconductor Division. In the glue-logic arena, the shift is from standard logic toward field-programmable logic and gate arrays for densities up to about 10,000 gates and standard-cell-based ASICs up to about half a million gates or so.


CREATING SHELLS FOR SOFTWARE

TI's Universe is a collection of software tools and programs that help programmers construct application shells for knowledge-based systems. Such customized software eventually evolves into a standard product.

TOOL SETS SPEED SOFTWARE DEVELOPMENT



Aimed at relieving the software "crunch," the Integrated Engineering Facility's integrated tool sets make for quick development of application software.

In processor design, Rhines says, TI is focusing on meeting the needs of three or four architectures. In the low end, it is tracking the IBM PC road map with specialized support-chip families. In both the 16- and 32-bit areas it has developed a four-chip family for EISA bus-based systems. This will be followed next year by specialized chip sets for 32-bit 386/486-based systems for digital signal processing, image and speech processing, and fax/modem transmission. Further out, around 1991, specialized chip sets will support token-ring networks and the Small Computer Systems Interface.

In the RISC and Unix market, he says, TI will move from just supplying support chips for the Sparc architecture to supplying a full range of products. By late next year, the company will be in production with a combined integer and floating-point unit, followed in 1991 by a single-chip processor that will also incorporate memory management and cache memory. In DSP, the company is continuing to make higher-performance and customer-specific versions of its TMS320 family as well as increasing throughput.

PARALLEL PROCESSING. Although the focus now is on consumer, automotive, and telecom tasks, future efforts will push for its use as a parallel-processing element in high-performance work stations and image processing. In embedded control, TI has focused on a configurable architecture based on the TMS370, which will allow generation of a diverse family of application-specific controllers.

By the mid-'90s, says Rhines, TI will be well on the way toward a silicon-compiler-based processor methodology, which will allow customers to "roll their own" by combining application-specific blocks developed for DSP, data-communications, imaging, and video applications.

The general-purpose logic marketplace is giving ground to ASICs, he says, a trend expected to continue in the '90s. Many logic parts, Rhines says, have been replaced by gate arrays and programmable logic devices. They substitute for small- and medium-scale-integration parts, while field-programmable gate arrays and standard-cell-based products replace LSI and VLSI peripheral logic. The highest growth, he says, is in support of emerging high-performance complex-instruction-set and RISC-based systems. To satisfy this requirement, the company has developed a three-pronged strategy: proprietary bipolar and CMOS PLDs specific to particular system requirements; programmable state-machine applications using EPLD technology acquired from Altera Corp.; and high-density VLSI/LSI logic replacement using the antifuse gate-array technology acquired from Actel Corp.

Memories will also follow an increasingly specialized road map, says Robert England, vice president and deputy manager of TI's MOS Memory Products Division. As the company moves beyond 4-Mbit DRAMs, these memories will become increasingly differentiated in modes such as page, nibble, and serial. Also, more specialized video RAMs and frame RAMs will emerge. Starting at the 16-Mbit level, England says, the focus at TI will be on smart DRAMs with multiple functional options and system-driven architectures. Similarly in erasable and electrically erasable programmable read-only memories, he says, with the advent of flash technology, specialized architectures will emerge at the 1- and 4-Mbit level, optimizing their architecture and speed for use in high-performance 32-bit processor applications.

The linear side is marking a similar trend, says Delbert Whitaker, senior vice president of the semiconductor group. There's a shift from commodity linear and even niche linear products toward what the company defines as advanced linear—application-specific mixed analog/digital circuits based on merged bipolar and CMOS processes.

Another growth area that TI is targeting is software development, with efforts ranging from providing integrated CASE tool sets—called "super-CASE" by TI—to developing complete applications for large customers by building on libraries of generic software "shells" for specific application environments. The challenge is to integrate an information system to serve the needs of all facets of an enterprise, says John W. White, senior vice president of TI's Information and Services Division. That includes management information systems, the factory operation, and irregular operations or operations management functions.

ENHANCED PRODUCTIVITY. "What's needed," says White, "is a CASE technology that allows us to characterize the total enterprise's business problem and to generate in the appropriate technology the applications to meet the enterprise's needs." Peter Van Cuylenburg, vice president of TI's Data Systems Group, predicts that in the 1990s the growth of networked systems will lead to more process-specific operations for management and for the shop floor, enhancing productivity much as spreadsheets and word processors did more generally in the 1980s.

"The next wave will be a much broader spectrum of specific applications," says Van Cuylenburg. "The previous wave was driven by a relatively narrow range of generic applications. The next wave will bring many applications useful to a relatively small group of people." Examples are airline operations, dynamic plant scheduling, hospital resource management, and service-bay operations.

In this environment, Van Cuylenburg points out, higher software productivity is essential. "We believe we have a recipe for the software-generation problem, a portfolio of tools to generate specific applications. Our object is to build a software business by providing this 'super-CASE' portfolio of tools. The approach is to take the 1980s software technology that has been developed and blend those together." These include integrated software engineering tools, artificial intelligence tools for developing application shells, hypermedia, object-oriented programming tools, and "semiconductor enablers for the new category of RISC-based high-performance work stations that these applications will be based on."

Key is object-oriented technology, which includes programming methods and data-base management. Object-oriented programming lends itself to modularity and reusabilty and is much easier to modify or customize than traditional process-oriented software, according to David L. Wells, a member of the technical staff at TI's Computer Science Center. A prototype of an object-oriented data base called Zeitgeist has been developed in the Lisp language and has been used at TI with VLSI CAD tools.

TI has ported a hypermedia system to the data base to support a relational query system as well. In development is a C++/Unix version that will become part of a software-development environment called Universe, another facet of TI's growing software business.

TI is using Universe to solve information-management problems for Fortune 500 companies while simultaneously developing standard products. Universe is basically a collection of software tools and programs that help programmers construct application shells for knowledge-based systems. For example, Universe contains network communications, relational data-base facilities, life-cycle support software, and other system tools.

Key to software is object-oriented technology, which includes programming methods that are better at customizing programs than are process-oriented approaches

For an industry segment—for example, airline scheduling—programmers develop a prototype program that applies to that general problem, and a domain knowledge base is built on that. For the individual customer, a custom code and custom knowledge base are added. "We try to separate out the domain knowledge and domain code from the custom knowledge and code, while the tool kits continue to grow as you learn from each application," says Don Oxley, manager of applications systems in the Data Systems Group.

The result is a structure consisting of tool kits on the bottom, domain code unique to an application, and other added knowledge (such as rules and heuristics that can be captured without having to write special code). At the top of the structure is some amount of unique code or knowledge that represents the customer's way of doing business.

The technique has been applied successfully to create a system for aircraft-gate assignment scheduling and display for United Airlines at O'Hare and Stapleton airports. The knowledge base and tool-kit know-how accumulated in these projects is being applied to other airline operations such as maintenance schedules at Air Canada and Iberia airlines. According to Oxley, these "domain capabilities" will eventually be extended to other arenas, such as health care.

TI is also developing a growing market for its portfolio of integrated CASE tools in a product called the Integrated Engineering Facility, or IEF. It is aimed at relieving the "software crunch," which, says Johnny Long, manager of market development for IEF, has evolved because software development takes too long, costs too much, and is usually poor in quality. Introduced commercially in late 1987, IEF became available as a complete product in March 1988. IEF consists of planning, analysis, and design tool sets based on AT-class 286/386 work stations, together with a complete code generator and data-base generator based on IBM mainframes. These are all integrated through local and central encyclopedias.

The tool kit automatically transforms data from the higher levels of abstraction and planning to the lower levels of abstraction required in analysis and design and finally to the detailed implementation built within the code and data-base generators. As a result, the tool set can provide a complete executable application-system generation. ☐

WHAT THE '90s HAVE IN STORE

By the year 2000, personal computers will have access to 100,000 times more data than today, thanks to networking and optical storage. Such "knowledge technologies" will come to the forefront as computing shifts from being process-centered to being knowledge-centered. So says George H. Heilmeier, senior vice president and chief technical officer of Texas Instruments Inc. Heilmeier also points to developments in six critical areas:

- Telecommunications: Intelligent networks will have knowledge-based network management. Local-area wireless communications will penetrate the low-speed LAN market leading to the wireless office and home.
- Automobiles: About $2,000 will be spent per car for electronics by 1995 (see p. 78). Autos will become mobile offices linked by fax and phone to home-office LANs.
- Manufacturing: The factory floor will be more customized, with shorter start-up times and production runs. Factories will have artificial-intelligence-based command, control, and communications systems. Brilliant systems will merge and interpret information from multiple sensors and manage their own operations by planning and acting.
- Consumer: High-definition TV will become a major market for analog-to-digital converters, video processors, memories. If the Far East doesn't dominate the U. S. market, work station and computer companies—rather than consumer—will be major players. To succeed in mass markets, system entry prices must be less than $2,000. Large displays, probably projection-type, will be imperative.
- Microelectronics: Chip-level performance will double, with the same design rules as today, based on biCMOS; at the system level, performance will double. Packaging density will be 50 times higher than that of surface mounting while manufacturing will be under 0.5-μm. Full-custom, million-transistor designs will take three months with three to five designers. Design automation will produce not only first-pass functionality but also first-pass parametrics, quality, reliability, manufacturability, and testability. Silicon and gallium arsenide functions will be married on the same chip.
- Knowledge technologies: PCs will go from handling the pencil-and-paper tasks of the modern office to a knowledge-access tool. Adaptive access to information will be a major issue. The ability to browse, manipulate, and retrieve will be simplified; trial solutions or a consulting function will be available. Knowledge systems will progress from smart to brilliant, capable of managing their own missions. This will be accomplished in real time. Hypermedia—multimedia presentation of information—based on object-oriented programming and data bases—will be the spreadsheet of the '90s. *–S. W.*

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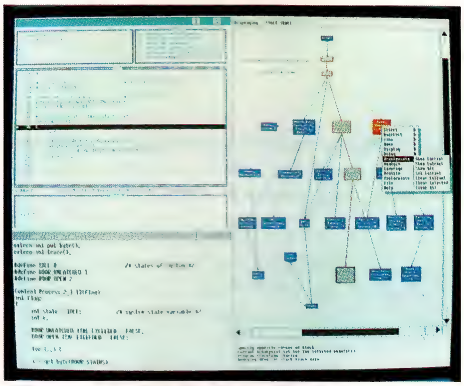
APPROACHING DUAL DESIGN

Mentor Graphics moves toward 'concurrent engineering' with a tool kit linking hardware and software design and debugging



The new tool set automatically generates a structure chart from C code.

Computer-aided software engineering tool kits typically consist of a hodgepodge of programs that perform isolated design-automation tasks but that don't necessarily work well together. Now, the leading vendor of design-automation tools has developed a CASE tool set that it says not only supports the entire software life cycle but also begins to bridge the gap between automated software and hardware design and debugging.

Mentor Graphics Corp. says its new CodeLink Station tool set represents a step toward what the Beaverton, Ore., company calls concurrent engineering—simultaneous, interactive, automated design of software and hardware. The set addresses software development from initial design through maintenance. It also tightly links software development with Mentor's hardware design-automation systems.

CodeLink Station gives users the industry's first solid link between a graphical interface and a debugging system. This link is provided by Structure Map, one of the tools in the CodeLink Station set. Structure Map automatically generates a software structure chart from source code that complies with the Institute of Electrical and Electronics Engineers 695A standard for the C programming language.

BY TOM MANUEL

Coupled with the Mentor hardware design environment, CodeLink greatly eases the tasks of writing and testing software. It also improves system efficiency; code is tuned to the hardware design because it is developed and debugged right along with the hardware. A direct link between CodeLink and QuickSim, Mentor's logic simulator, lets designers test code on simulated hardware. Development teams can make critical software and hardware design trade-offs early in a project—before changes become very costly.

BITS AND PIECES. "In recent years, software designers have been offered CASE tools in bits and pieces, resulting in a fragmented and sometimes isolated design environment," says Gerry Langeler, president and chief operating officer at Mentor. "The front-end CASE solution is an incomplete answer to the embedded-software bottleneck."

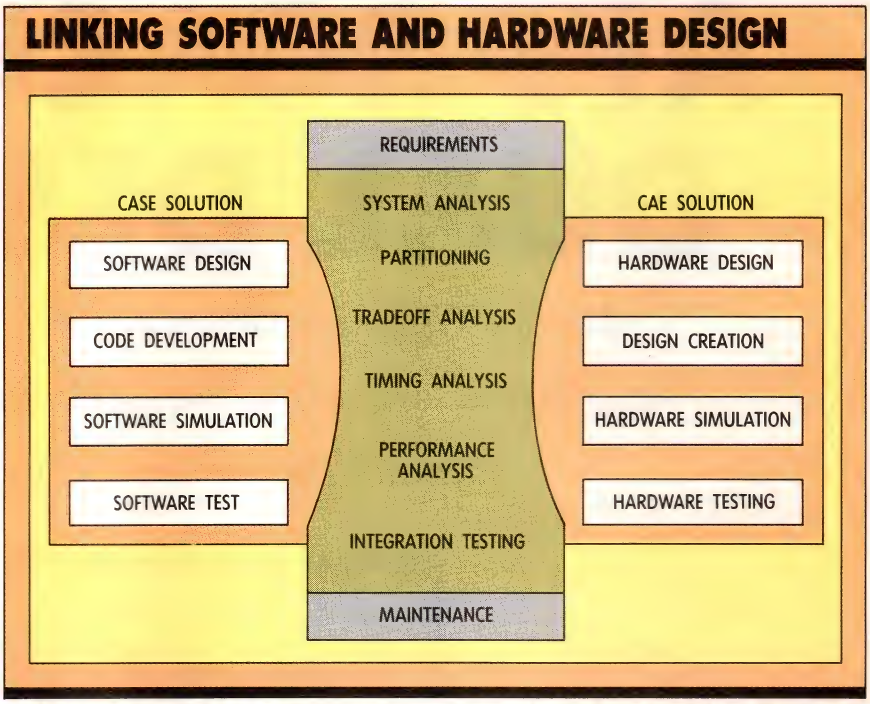
While the hardware development process has matured significantly in the last few years, Langeler says, software development has not. "Software development is in the critical path for project completions in the 1990s," he asserts. CodeLink, he says, is Mentor's answer to the problems of software development for embedded systems.

CodeLink's chief benefit lies in enabling software developers to take a very early and active part in system design, letting them work hand-in-hand with hardware designers. With CodeLink, software engineers can evaluate their code on the target hardware much earlier in the design cycle than previously possible. This eliminates much of the bottleneck currently experienced in the systems integration and debugging processes. CodeLink allows code to be developed and debugged before the integration stage is reached.

CodeLink performs behavioral and timing analyses as it runs code on the virtual target hardware through QuickSim. Mentor has linked the software development environment directly to QuickSim's instruction-set simulator. As software executes on the simulator, events on the processor's input/output lines are translated into the appropriate signals and states for input to the hardware design. A functional model of the system bus and processor serves as the link between the hardware simulation and the instruction-set simulator.

CodeLink lets software engineers debug at a higher level of abstraction than the code level while maintaining line-level capabilities for analysis. CodeLink's debugger can be used to evaluate code within three versions of the target system. Those versions are native mode, virtual mode, and physical mode.

In the native-mode version, code is executed on the host processor of the development work station. In virtual mode, code runs on simulated hardware. The physical mode involves execution on prototype target hardware. A common user interface makes it easy to debug code in all three modes.



Tightly coupling CASE and CAE is Mentor's goal in devising CodeLink Station; it lets hardware and software engineers make critical design trade-offs early.

CodeLink promotes an open interface by supporting the IEEE 695A standard as a compiler interface. Users can employ their favorite C compiler as long as it complies with that standard. Software engineers can introduce existing source code into the system, generate a structure chart, and incorporate old code into new systems. With this feature, CodeLink greatly facilitates code reusability—a major consideration for future software design efforts.

CodeLink's Structure Map component automatically generates a detailed structure chart from C source code. The structure chart shows the program's major modules and software flows, giving the software engineer an easy-to-follow high-level graphical understanding of how the program works. For some source code, the structure chart generated by CodeLink is the most succinct documentation, if not the only available information on the program's design.

Among the detailed information displayed on the structure chart is code performance and complexity. This information is displayed next to the relevant modules so that the software designer can see at a glance relationships among these measures, as well as the structure of the overall program. Such insights are critical for rapid debugging.

CodeLink can also be configured to filter its information to simplify code analysis and debugging. For example, the programmer can select a range of parameter values or a set of software modules that CodeLink is to report upon on the structure chart. The software engineer can then focus on those elements by viewing an uncluttered structure chart. As another example, all modules with code coverage under 10% can be highlighted to indicate low test coverage or even unexecuted code.

Even furthering the debugging process, portions of the actual code can be listed in pop-up windows next to the corresponding modules in the structure chart for line-by-line viewing and modification. A stack-trace feature highlights the sequence in which modules are executed and the data flows that lead to a particular user-defined event. This feature simplifies the debugging process in embedded systems and helps the software engineer make more efficient use of software design methods.

Mentor's debugger is based on the popular X-Ray debugger developed by Microtec Research Inc. of Santa Clara, Calif. The X-Ray debugger links to many popular hardware emulators for embedded processors, including the diverse line of emulators from Hewlett-Packard Co. of Palo Alto, Calif. This family includes the HP64700 series, which supports Motorola Inc.'s 68000 and 68010 chips along with Intel Corp.'s 8086, 8088, 80186, and 80188 processors. ☐

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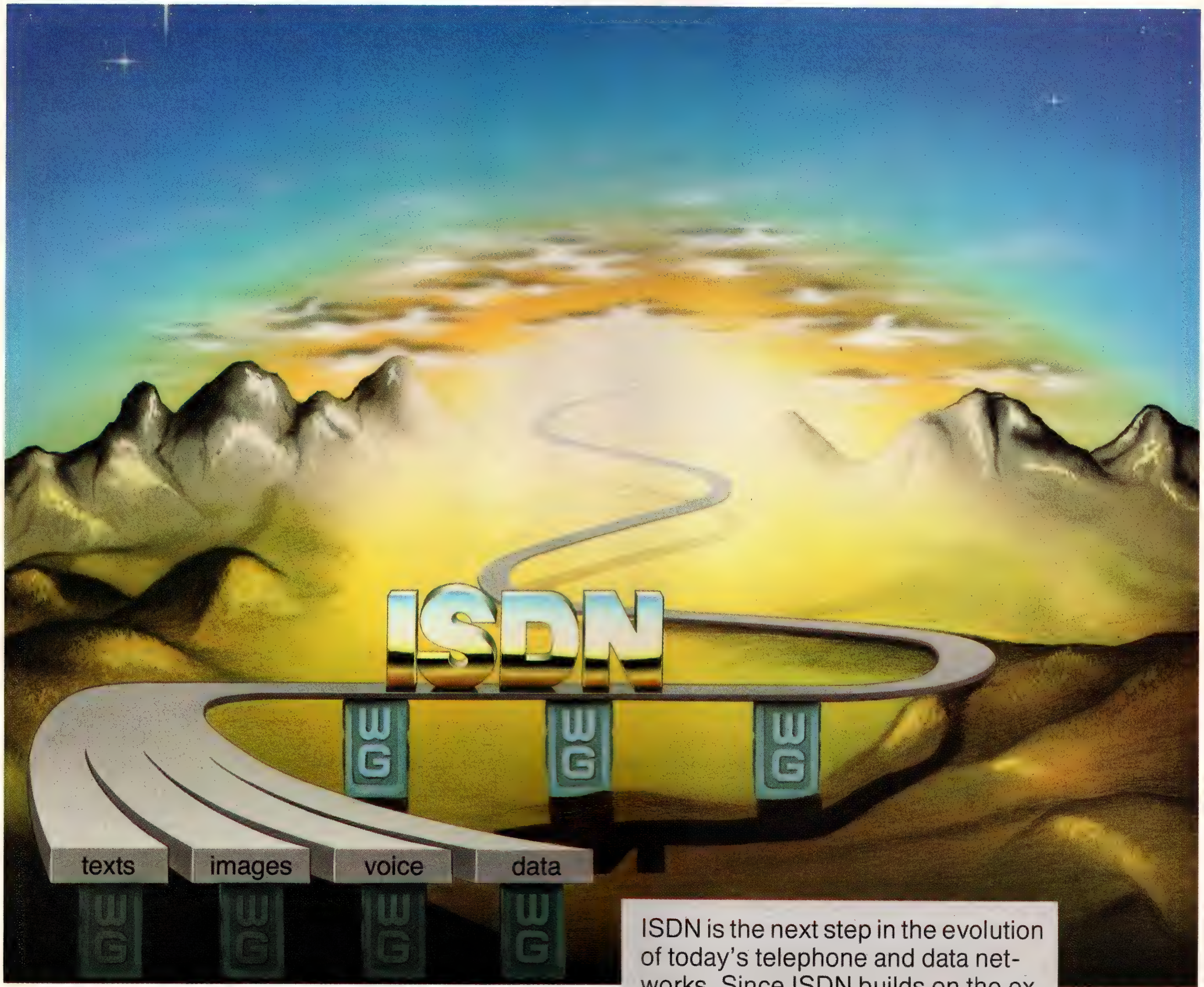

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Circle 205

IMAGING AND GRAPHICS MERGE

An imaging board that teams high resolution and real-time image processing can turn a PC into a graphics work station

BY

LAWRENCE CURRAN

The Image series from Matrox Electronic Systems Ltd. is more than just the logical next step up in resolution from its forerunner, the MVP-AT image-processing board for IBM PC ATs. Matrox's next-generation family of boards for the first time combines high-resolution graphics with real-time image processing in an expandable, integrated product line.

The new family brings 1,280-by-1,024-pixel, 32-bit resolution to AT-based image processing—a realm still dominated by 640-by-480-pixel, 8-bit applications, which the MVP-AT serves. The board family is built around Texas Instruments Inc.'s TMS34020 graphics microprocessor and TMS34082 floating-point coprocessor, which enable imaging functions to run 2 to 10 times faster than with the MVP-AT. Also on the boards are "all the functions that today's boxed image-processing systems do," says Lorne Trottier, president of the Dorval, Quebec-based company.

The Image series subsystem converts a personal computer into a much more versatile imaging work station than is possible using current board-level products, says Danny Mueller, a Matrox integration specialist. That's because it combines an intelligent subsystem controller—the TMS34020—with a modular hardware architecture, high-level software tools, and high-speed graphics.

Real-time image processing is the ability to process 30 frames of 512-by-512-pixel data per second. The Image series achieves a 15-MHz processing rate, which translates into some 50 frames/s. "That speed means that the new family's hardware execution time for a three-by-three convolution—a typical function—is one frame time, compared with 10 frame times for the MVP-AT," Mueller says.

Mueller notes that graphics are becoming increasingly important in image processing; that's the forte of the TMS34020 graphics engine, whether the task is as simple as annotating images or as complex as implementing user interfaces, such as X Windows. "Image-processing boards usually require a user to sacrifice part of the image buffer to handle graphics overlays. We overcome this by using a separate overlay buffer for graphics," he says.

Further, graphics drawing should be very fast to accommodate an interactive-windowed interface, Mueller says. "When the user re-sizes a window, it should happen immediately," he says. "Similarly, the display must be able to draw in the overlay buffer while images are being processed in the image buffer." Use of the graphics engine and coprocessor, along with Matrox's library of high-level graphics primitives, meets those needs, Mueller says.

The initial three boards in the family go into AT-host work stations and systems for applications including medical imaging, printing and publishing, satellite imaging, training, and simulation. The display board (IM-1280) is the intelligent subsystem and display controller, delivering 1,280-by-1,024-pixel, 32-bit resolution. It incorporates the TMS34020 32-bit graphics processor and TMS34082 floating-point unit. Another version of the display board is available for 640-by-480 applications. The IM-ASD monochrome acquisition and digitizer module and IM-RTP real-time processor round out the subsystem. The first addition to the board family will be the IM-CLD color-acquisition and digitizer board, to be released in March.

The TMS34020 is the subsystem's central processing unit, performing command interpretation, interrupt-driven processing-hardware control, and graphics generation. Depending on the display board version used, the display resolution can be customized to provide either a landscape format of 640 by 480 or 1,280 by 1,024 pixels, or a portrait format of 1,024 by 1,280 or 480 by 640 pixels. The board also provides for European display formats under software control.

Besides the TMS34020 and TMS34082, the display board incorporates two types of buffers, local random-access memory, and the RAM digital-to-analog converters that directly drive the display and three gate arrays. One buffer measures 2,048 by 1,024 pixels by 4 bits to handle graphical overlays. Four main frame buffers measuring 1,024 by 1,024 pixels by 8 bits store digitized image frame data. The main frame buffers can be reconfigured under software control, creating, for instance, 32-bit buffers for true color applications.

One of the CMOS gate arrays, the SDP-1024, is a serial data processor. It controls data distribution over the subsystem's internal expansion bus, "acting as the interface device between the frame buffers and the outside world," Mueller says. Another, the ADR-1024 address generator, produces four sets of processing addresses simultaneously for the main frame buffers and two sets of display addresses for the overlay buffer. The third gate array, the VDO-1024, acts as a multiplexer to provide display data to the RAM DACs.

Discussing the IM-1280, Mueller says it's essential that the baseboard have a local CPU "so that it can manage the imaging subsystem and offload the host CPU." For example, he says, the application software running on the host CPU has to decide what action should be taken as the result of a statistical operation, such as a histogram. "But the host CPU shouldn't be burdened with calculating the histogram," Mueller says. "That's the responsiblity of the image-processing subsystem."

The TMS34082 floating-point chip complements the CPU by being well suited to number crunching. It can draw in 4-, 8-, 16-, and 32-bit formats in either of the two types of buffers, ensuring high-speed drawing.

Before any such operation can take place, however, the images must be acquired and digitized. That's the function of the IM-ASD monochrome module and of the planned IM-CLD color-acquisition module. The monochrome unit takes inputs from any analog source that operates at up to 15 MHz, including RS-170 cameras. It can also take input signals from any digital source at up to 30 MHz.

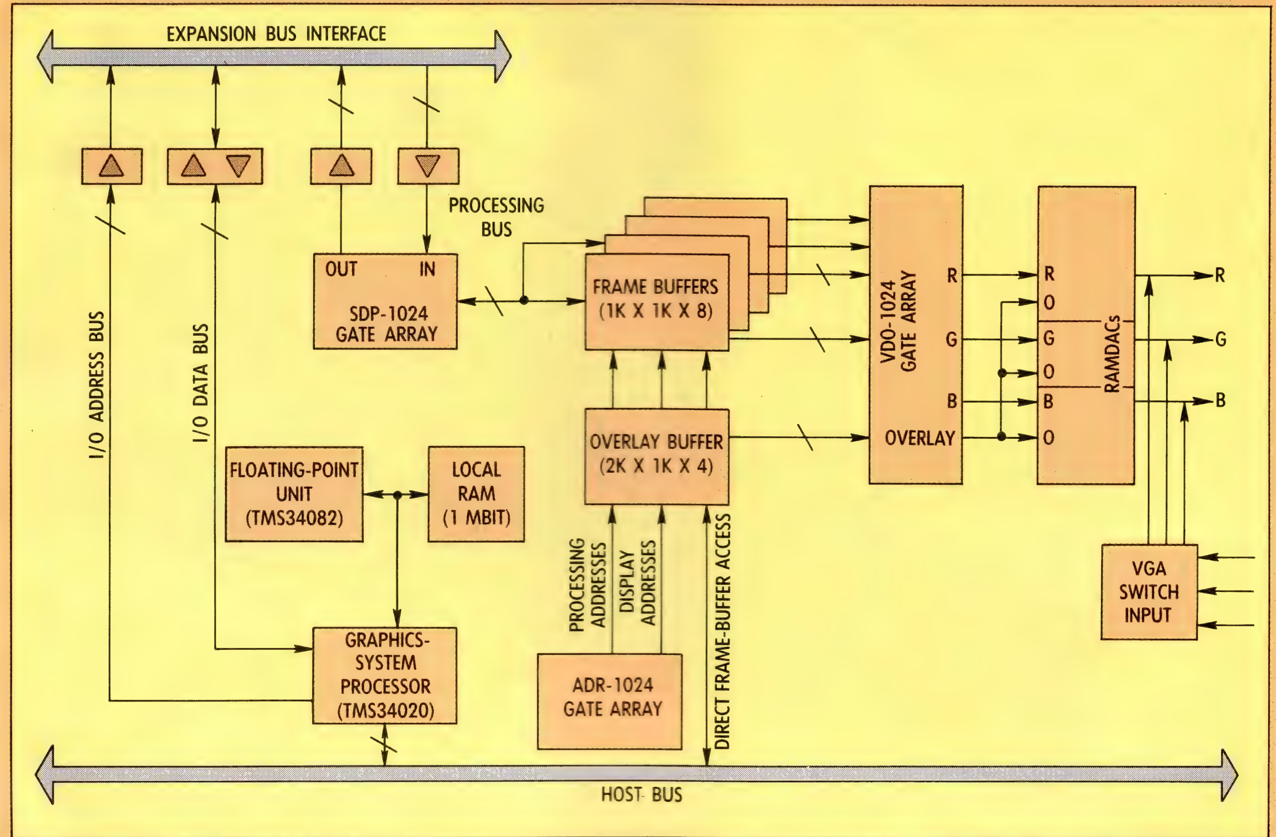
Finally, the IM-RTP board rounds out the subsystem. It's the real-time image-processing heart of the Image series, controlling such functions as point-to-point transforms; spatial filtering, including convolutions; binary, gray-scale, and high-level morphology; statistical functions, such as histograms; and object analysis. The board can process data directly from the digitizer boards or the frame buffers at 15 MHz.

A two-layer software approach in the Image series simplifies things for application programmers. Board-resident software runs on the local CPU—the 34020. A host layer runs on the host processor. Code that runs on the local CPU performs the graphics, image-processing, acquisition, and display functions. Host-resident code issues commands to the 34020 by means of a memory-mapped command first-in, first-out register on the display board. The 34020 then interprets the commands for execution by the imaging subsystem.

Matrox's expansion bus carries high-speed subsystem communications. That bus has both an input/output channel and a processing channel. The 34020 uses the I/O channel to initialize and control any add-on boards still to come in the Matrox family or custom boards added by users.

The processing channel includes a dual 32-bit data bus with a peak frequency of 30 MHz. Data flows synchronously frame by frame between digitizers, image memories, and processing boards. ☐

HOW MATROX PUTS ITS DISPLAY BOARD TOGETHER



Matrox's display board, an intelligent subsystem and display controller, delivers resolution of 1,280 by 1,024 pixels by 32 bits. It incorporates the TMS34020 32-bit graphics processor and TMS34082 floating-point unit.

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COMPANIES TO WATCH

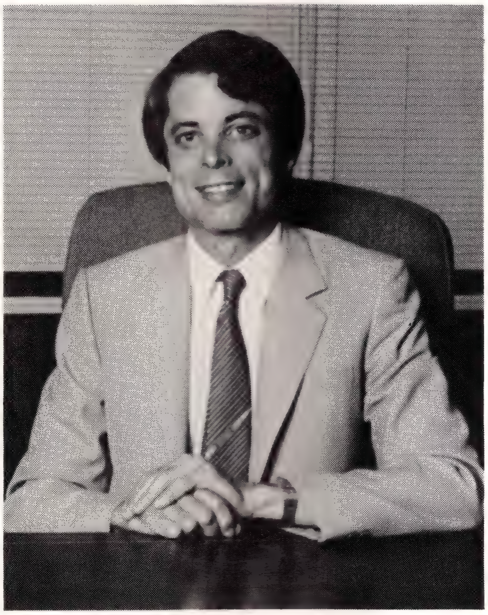
MATROX CONJURES IMAGES OF A $250 MILLION FIRM

Steady 35% growth would put it there in 1994

DORVAL, CANADA

On a mild Friday afternoon last April, Lorne Trottier gathered some 550 of his employees into the company cafeteria to tell them the good news: Matrox Electronic Systems Ltd. had just completed another outstanding year. Revenue for fiscal 1988 had soared to $66.5 million from $40.8 million in U. S. dollars. Trottier, who is president, didn't say so then, but he believes Matrox will become a $250 million public company in five years.

That would make for ever bigger semiannual wine-and-cheese parties at Matrox, a manufacturer of graphics and image-processing boards based in the Montreal suburb of Dorval. At these shindigs, the low-keyed Trottier shares financial results with employees, announces the amount of the profit-sharing pool, hands out prizes, and thanks everyone for contributing.


President Lorne Trottier says Matrox is reaching for new graphics and image-processing markets.

Trottier's growth scenario is not farfetched. Matrox has been profitable for all of its 13 years of existence, marking a compound annual growth rate of about 35%. Trottier cofounded the company in 1976 with fellow electrical engineer Branco Matic, who is now chairman of the board and head of strategic planning.

Matrox is reaching for new markets with its latest family of image-processing boards for IBM AT-compatible personal computers (see p. 102). The Image Series—which Trottier says rivals much pricier boxed imaging systems and boards from competitors—melds 1,280-by-1,024-pixel graphics with real-time image processing. In effect, it transforms a PC into an imaging work station. With the Image Series, Matrox is aiming for a bigger share of high-performance medical applications.

Imaging contributed about $10 million to 1988 sales, a portion that Trottier expects to double as the Image Series takes off. Of the remainder, graphics represented some $26 million, interactive video-disk delivery systems $20 million, and financial-information displays for stock-quotation systems $7 million. Miscellaneous activities accounted for the rest.

To date, Matrox's main business in video-disk delivery systems has come from a U. S. Army contract to provide training systems. They consist of a PC AT-compatible computer and video-disk player that presents information to students in text, graphic, and analog or digital audio form. The contract will be worth $80 million to $90 million to Matrox overall.

For financial applications, Matrox provides video controller boards for alphanumeric displays used in stock-quotation systems. Trottier expects that both the financial business and the video-disk segment will hold steady in 1989.

The big growth will come from the medium-to-high-resolution graphics segment—32-bit systems with 1,024 by 768 or 1,280 by 1,024 pixels—along with the image-processing niche Matrox has carved out for itself. In imaging, it offers products that support the major buses used in industrial and medical applications including the Q-bus, Multibus II, STD bus, VMEbus, and the PC-AT.

The emphasis on high-performance products puts Matrox in competition with companies such as Control Systems, Number Nine Computer, and Vermont

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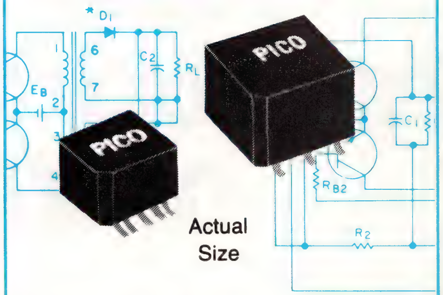

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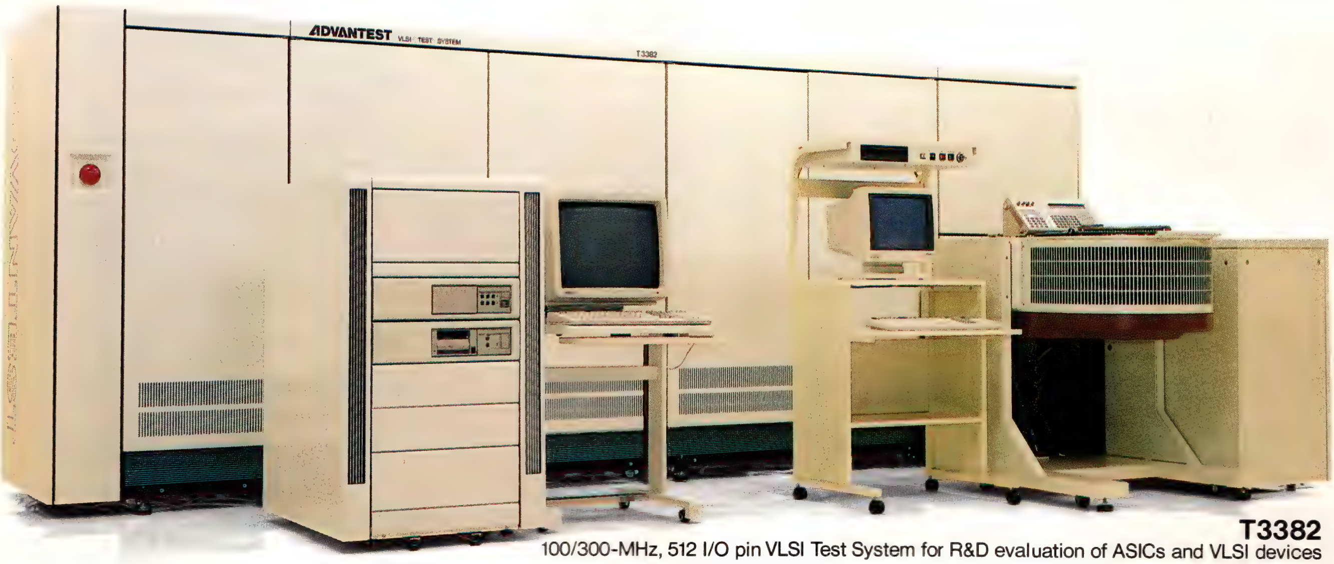

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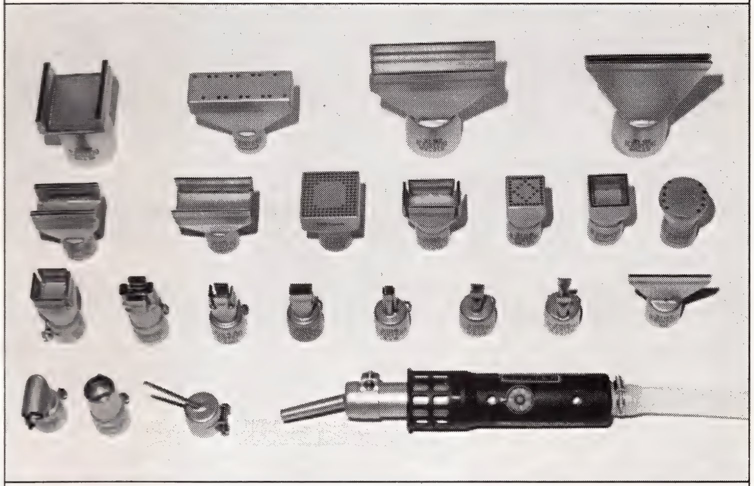

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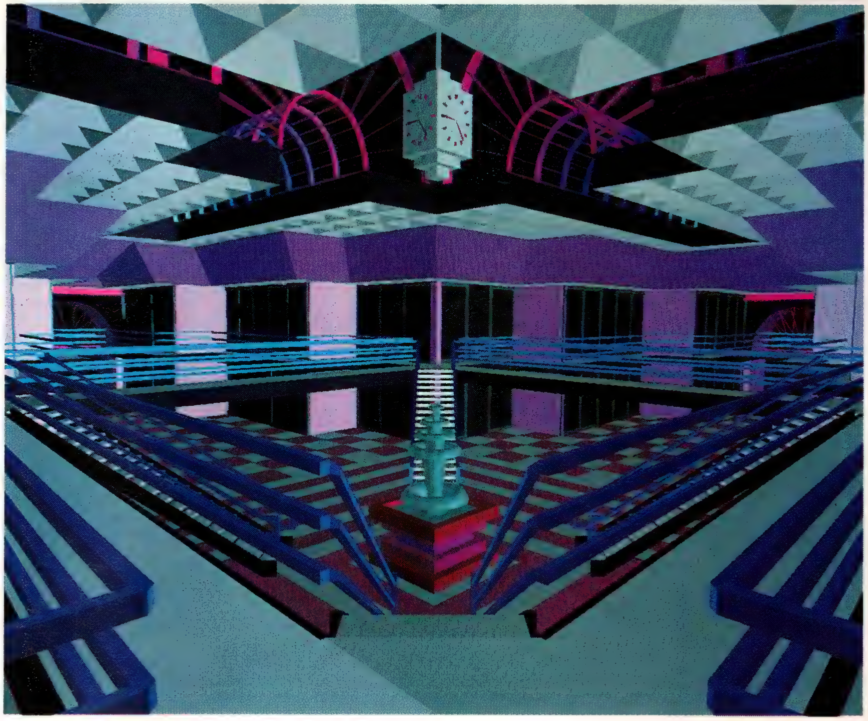

A Matrox board produces CAD output based on the Autoshade program, part of the popular AutoCAD package for designing mechanical parts from Autodesk Inc.

Microsystems in graphics, and with players such as Datacube Inc. and Imaging Technology Inc. in image processing.

Trottier claims the Image Series offers major advantages over Datacube and Imaging Technology board families. The Matrox solution, he says, will have "a lot fewer boards at a lot less cost" than the competitors. The Image Series core set "does in three boards most of the functions, plus some additional algorithms, that those other families do in 12 to 20 slots."

ASIC DESIGN. That functionality stems in part from a strong application-specific integrated circuit design capability Matrox has developed, according to Trottier. The firm has invested more than $2 million in ASIC design tools, so "every new product we do incorporates one or more gate arrays to give more functionality at less cost," he says.

One authority on graphics and imaging thinks that Matrox has done a good job of learning what the market wants, then providing it. "They've responded to the market with high-resolution graphics boards and seem determined to stay on the leading edge," says Joel Orr, president of Orr Associates Inc., a Washington, D. C.-area consulting firm.

Matrox products, Orr says, "have been carefully refined in the crucible of CAD usage." They have come through, he says, "at a much higher level of purity than those of companies that haven't sold as many [boards]."

Future graphics products will include a strong emphasis on high-performance boards for work stations, such as the 1,280-by-1,024-pixel board Matrox supplies as a high-resolution option to the Apollo Division of Hewlett-Packard Co. Those boards are used in Apollo's Series 3500 and 4500 two- and three-dimensional graphics work stations. "We want to do more OEM business in the work-station area," Trottier asserts.

The company is also going after a couple of markets that are new for Matrox: video graphics and dealer-channel CAD. Trottier describes video graphics as a form of graphic arts, but requiring more bit planes—16, 24, and 32, compared with 8 for traditional graphic arts—to provide true color images. "We hope to announce some products in this area in the next year," he says.

In the dealer channel, which the company hasn't addressed to date, Matrox is developing products that are intended to gain "a significant share" of the PC-based AutoCAD dealer business. AutoCAD is a widely used software package for designing mechanical parts from Autodesk Inc. of Sausalito, Calif.

"We're in the video microtechnology business," Trottier says, defining that as encompassing any board or interface "that marries video to a microcomputer." In that context, "we're trying to build the areas where we're currently active and strong as well as identify some new market segments," Trottier says.

Along the way, he hopes to maintain the company's historical annual growth rate of 35%, which would catapult Matrox to $250 million or $300 million in annual revenue by 1994. "Ultimately I'd like to see Matrox as a public company," Trottier concludes. Based on the record to date, don't bet against all of that happening. *–Lawrence Curran*

IN THE COMING SHAKEOUT, THE BETS ARE ON BULL

MILAN

European computer makers have grown fat off the virtually captive markets in their home countries, but the day of reckoning is fast approaching.

Changes in the business are squeezing profits, and many analysts agree that a shakeout is coming, with only a couple of vendors expected to survive. Already, Bourses from Milan to Munich are abuzz with rumors about possible mergers between companies as diverse as West Germany's Siemens AG and Italy's Ing. C. Olivetti & Co.

But one company that is rarely mentioned in the merger and buyout rumors is France's state-owned Compagnie des Machines Bull. The analysts say that Paris-based Bull has the three qualities needed to survive: products, distribution, and access to cash. Each of the other national champions lacks at least one of those qualities, they add.

"From 1982 to 1988, Bull president Jacques Sterns made the right choices," says Georges Chretien, an analyst with the Stanford Research Institute in Paris, "and I think that the company is ready to face the hardships of the next two years." One of these choices was the acquisition last year of all of Minneapolis-based Honeywell Inc.'s computer operations. Bull spent $200 million to buy the former Honeywell Information Systems' computer manufacturing, research and development, and marketing operations. (Honeywell retains a 15.2% stake in the Boston-based Bull HN Information Systems Inc., and Japan's NEC Corp. has another 15%).

The purchase—a surprisingly aggressive move for a state-owned company—brought Bull to the top of the list of the European-based suppliers of information technology, with sales of $5.3 billion in 1988. "Bull is the most geographically diversified of all the European computer companies," says George Verghese, an electronics industry analyst with Deutsche Bank in London. "The Honeywell purchase gave the group a solid presence in the American market."

With margins disastrously low on personal computers, Bull has the advantage

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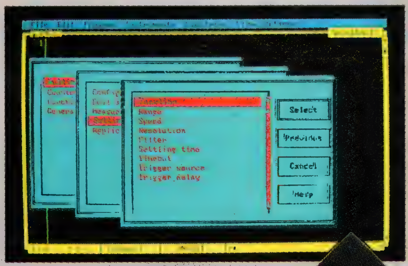

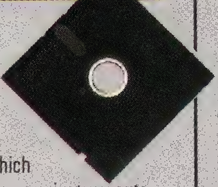

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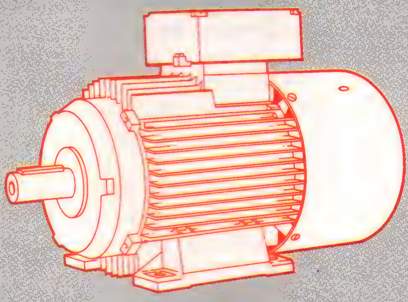

A company in The Netherlands has built a GPIB system for testing motor control printed circuit boards. The boards are built into a VME rack system used to control the heavy electrical motors in trams and trains.

This application uses two Fluke 8840 multimeters for various measurements on the PCBs. In this case the speed of data transmission over the system bus was the main reason for choosing the Fluke 8840.

Spotlight on Multimeters

The range of multimeters now offered by Fluke and Philips is one of the most comprehensive from a single supplier.
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of a good reputation as a producer of mainframes and minicomputers. "There aren't that many mainframe producers left [in Europe], and many customers need these machines to run those large networks," says analyst Chretien.

But Bull hasn't had everything its way. The company has been hurt in Europe and elsewhere by its reliance on its proprietary GCOS operating system for its mainframe and minis. However, Bull has already brought in a range of Unix-based products integrating X/Open standards.

Like all the major European producers, Bull reorganized last year, cutting about 1,500 jobs to bring worldwide employment to 44,000. Analysts expect it to continue to slim down in the coming year. "Bull still has too many layers of management," says Dennis Exton, industry analyst with UBS-Philips and Drew in London, "so that it's important to continue the restructuring process."

What Bull has, that many of its competitors do not, is access to state capital. The French government owns 90% of the company, with the remaining 10% available to investors only in the form of participation certificates.

The French government is currently dominated by the Socialist party, which opposes privatization. "That means," says one French analyst who prefers not to be identified, "that the French government is not going to forget about Bull."

And it hasn't. At the end of 1988, the government gave the company $167 million as part of a capital-boosting operation. The company is expected to raise more funds this year.

Having a shareholder with deep pockets may be even more important for Bull now. Though the company predicts a small profit in 1989 after 1988's $45 million, analysts are doubtful it will be able to reach that goal. In the first six months of 1989, the company posted a loss of $77 million while sales grew only 1.5%. Bull is blaming the loss on production difficulties that made it late in supplying products to its customers.

"But every [computer] company had bad results this year," says analyst Chretien. "It is the next two years that will tell the tale for the European-based original-equipment manufacturers." And Bull, he says, "seems a likely candidate to make it through." *–Andrew Rosenbaum*

AT ANALOG DEVICES, THE FOCUS IS ON PROCESSES

NORWOOD, MASS.

Having a sophisticated repertoire of process technologies is one of the key ingredients for semiconductor manufacturers that hope to stay in the race as suppliers of analog and mixed-signal (analog and digital) integrated circuits. That message hasn't been lost on strategists at Analog Devices Inc.

The $440 million Norwood, Mass., company has come a long way in the short time since it introduced the industry's first true monolithic 12-bit analog-to-digital converter in 1985. The AD574 was built with an integrated-injection-logic bipolar process, and it's still made that way. But today there is a lot more in the company's bag of process and circuit tricks.

Analog Devices has been investing some $10 million a year since 1985 in process development for its three fabrication facilities. The investment is paying off in high-speed ADCs, multipliers, and amplifiers—products that operate at greater than 100 MHz where earlier processes topped out at about 80 MHz. In fact, says Jerry Fishman, group vice president for components, the company will have introduced some 370 new products between 1988 and 1992, with more than 50 unveiled last year alone. They will contribute 1992 revenues topping $100 million.

Several processes are running or in development, but two in particular have contributed to the specs of recent high-performance products: Flash and complementary bipolar (CB).

Flash is a 4-GHz bipolar npn process using double-level metalization and laser-trimmed thin-film resistors. That combination results in stable and predictable currents in bias circuits, along with an ability to compensate for temperature variations in gain and comparator offset.

FLASH PRODUCT. The AD834 multiplier, a Flash-produced product introduced last November, takes two analog signals ranging from dc to 500 MHz and produces an output that is the product of their multiplication. Previous units couldn't handle signals much above 80 MHz.

The CB process overcomes the inherent limitations on analog designs imposed by existing bipolar processes, especially the slowness of the pnp transistor. Cutoff frequency was typically 10 MHz in devices that had npns with cutoff frequencies up to 400 MHz.

The CB process yields pnp transistors with cutoff frequencies of 700 MHz and npn versions at 600 MHz. It's done by combining ion implantation for up-diffusion with conventional down-diffusion on a p-epitaxial process.

There's more to come. Waiting in the wings is Abcmos, for advanced biCMOS, which promises blinding speed in data converters. *–Lawrence Curran*

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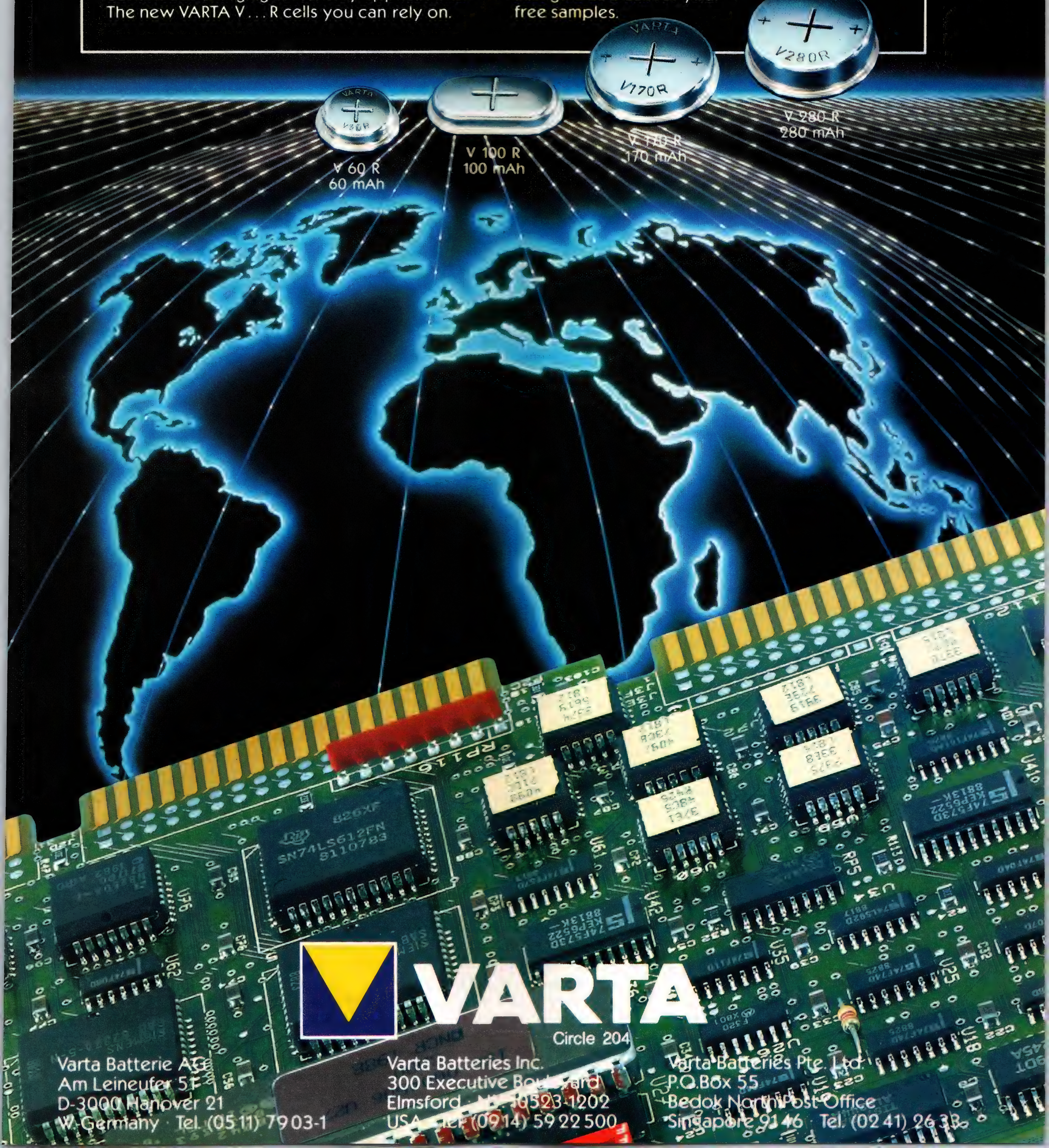

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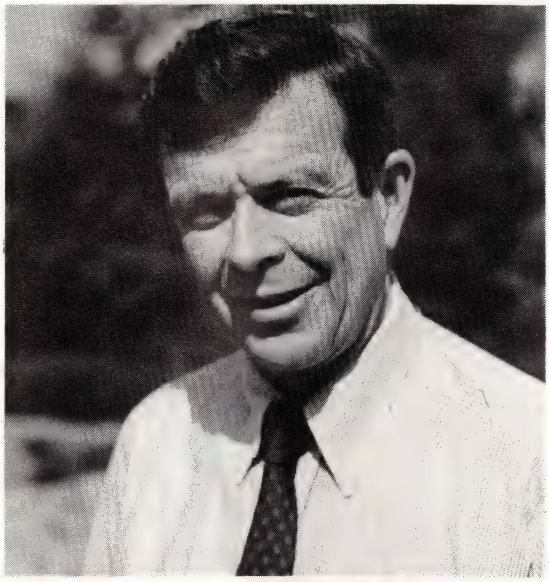
PEOPLE TO WATCH

SPRAGUE'S GOAL: TURNING R&D INTO PRODUCTS FASTER

The semiconductor veteran, now a consultant, says Japan does it better

LEXINGTON, MASS.

Paul Revere passed through Lexington on his 1775 ride from Boston to Concord to warn the colonists that the British were coming. Now it's John Sprague's turn to alert the electronics community that another invasion is advancing—from Japan.


Consultant John Sprague says the U. S. can learn some lessons from the Japanese about applying R&D spending.

Sprague, the president of John L. Sprague Associates, a Lexington-based industry consultant, says technologies developed in Japan get into consumer and industrial applications very fast. The 59-year-old former president and chief executive officer of Sprague Electric Co. wants to show U. S. companies how to get similar results.

Sprague works with clients as a technology analyst, applying his experience in research and development and manufacturing to evaluate an idea's potential for early commercialization. He also acts as a bridge between client companies and others that may benefit from some kind of affiliation—a development contract, joint venture, or acquisition. His early focus is on products or processes using advanced materials for electronics, especially ceramics.

Between 1959 and 1968, Sprague—who holds a PhD in physical-inorganic chemistry from Stanford University—was closely involved with R&D at Sprague Electric. Among other posts, he was senior vice president for engineering and for R&D, and senior vice president of the Semiconductor Division in Worcester, Mass. The division was a pioneer in chip doping using ion implantation and now supplies parts for automotive and industrial products.

Sprague became president in 1976, resigning two years ago to set up a consulting business "because of a greater personal interest in technology management than in general management."

MATERIALS. One client to date is Charles River Associates, a Boston economics, engineering, and management-consulting firm that has a strong materials group, Sprague says. His project involves sensors made "with very advanced materials. I'm trying to define the segments this client should invest in."

In that effort, Sprague brings to bear his knowledge of sensor use in automobiles—a major application opportunity. Sprague talks with Charles River materials scientists to understand the scope of their work, then surveys the literature to find out what's been published on sensors, "helping to sort out which directions have commercial potential.

"Then I'll talk to people in the commercial electronics world, possibly to set up an acquisition or joint venture" that would involve Charles River through one of its clients. Those clients include venture capital organizations seeking help in assessing technologies as investment opportunities.

Sprague cautions that U. S. companies face formidable obstacles to quickly commercializing their technology. These include the traditional serial way developments move from invention to production, a short-term focus on financial results, and a "not-invented-here" attitude.

Sprague has firsthand knowledge of Japan: he served as a director of Nichicon/Sprague Corp., a joint venture between Sprague Electric and Nichicon Capacitor Corp., a Japanese manufacturer of tantalum capacitors in Kyoto. The Japanese approach R&D as a commercial venture, he says, while in the U. S., about half of the $130 billion spent on R&D is federally funded. As a result, sophisticated materials work at universities and R&D facilities is channeled into military applications, with their agonizingly slow development and product cycles.

The Japanese manage to sidestep this lengthy process, which involves discrete steps from invention to prototyping then production. Sprague contends that "if the user of a process isn't almost in on the invention, which is typical in Japan, the process probably won't work in production."

The other Japanese methods that can be helpful are comprehensiveness, persistence, and an emphasis on built-in quality. "Japanese science is thorough. They absolutely understand a process before they put it into production. They're also persistent; they stick with it for the long term," he says. Too often, U. S. management has to focus on the short term because of the pressure of quarterly financial results and a need to show early returns on investments in technology.

As for the not-invented-here factor, Sprague cites an example that illustrates the need for U. S. firms to change. He learned that Japanese manufacturers of mobile phones were using lithium tetraborate as a surface-acoustic-wave filter material; U. S. companies use quartz. When he asked representatives of some of the U. S. companies why the Japanese used a different material, the response was often "we don't know and we don't care." In contrast, "Japan doesn't have a problem about learning from others," he points out.

Eventually, Sprague hopes that more U. S. jobs will flow from the work of John Sprague Associates. "I'd like to help create jobs in the U. S. that result from the commercialization of U. S. technology," he says. "I wouldn't mind if that results, in part, from foreign investment in the U. S." *–Lawrence Curran*

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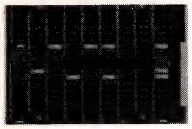

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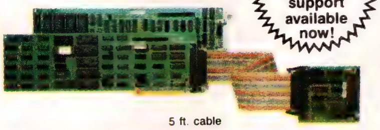

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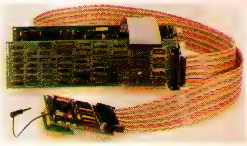

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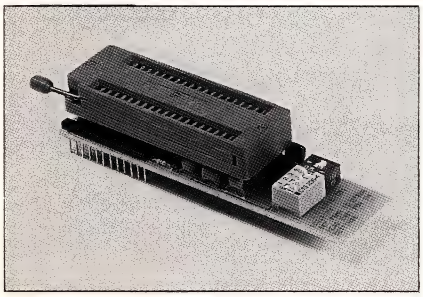

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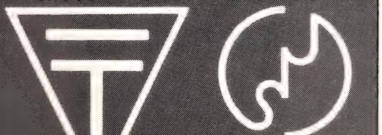

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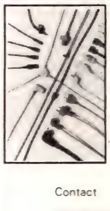

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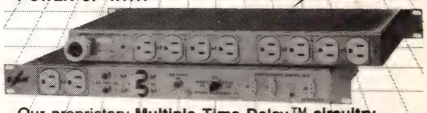

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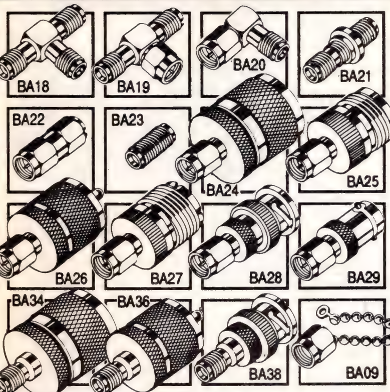

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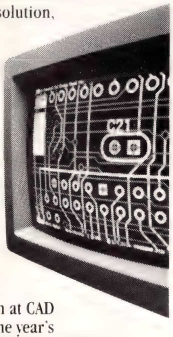

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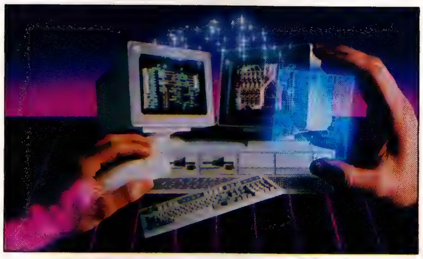

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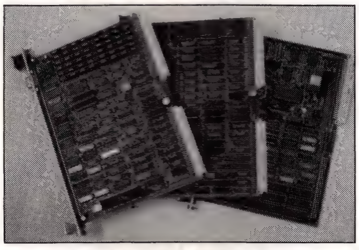

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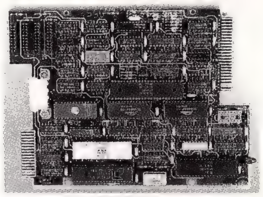

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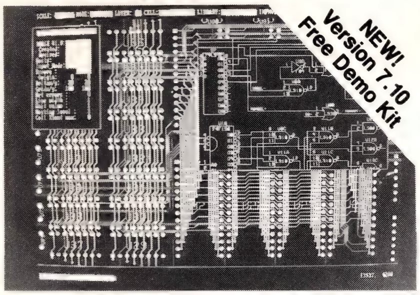

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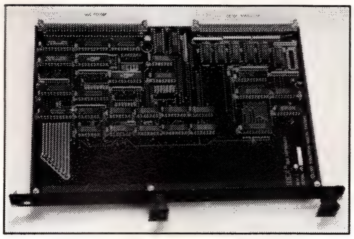

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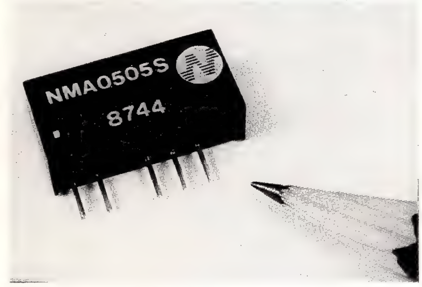

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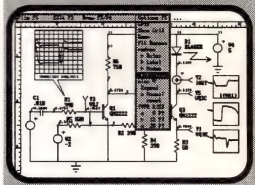

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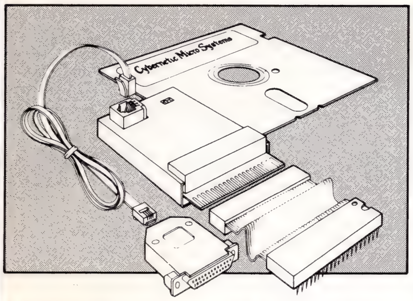

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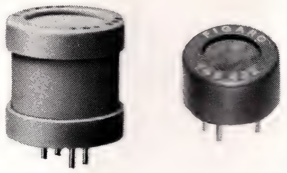

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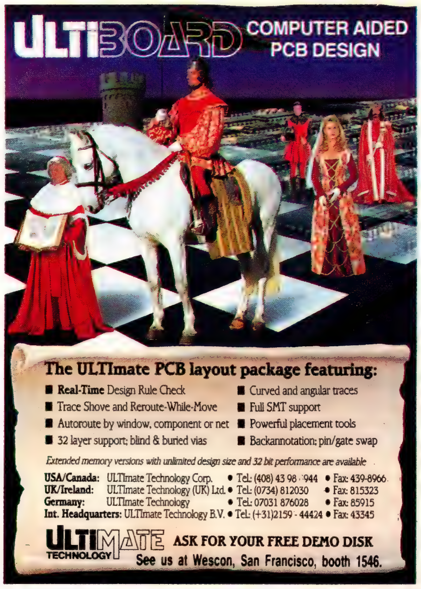

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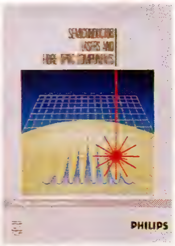

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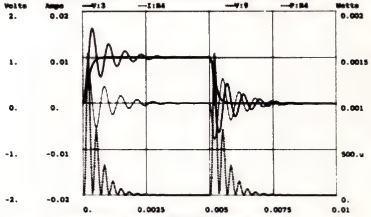

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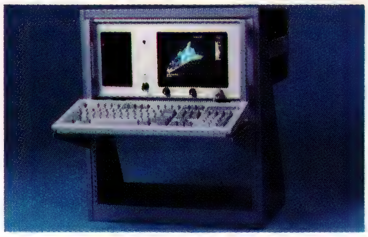

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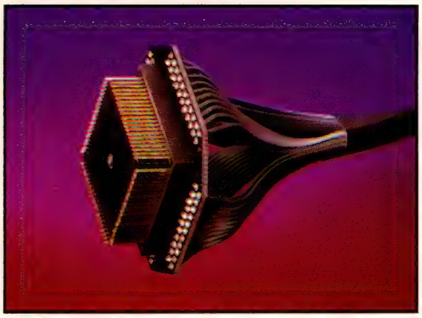

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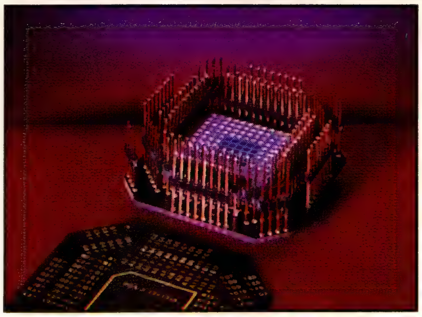

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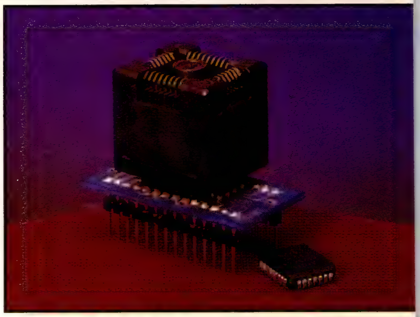

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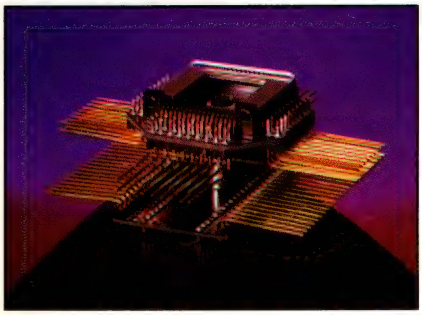

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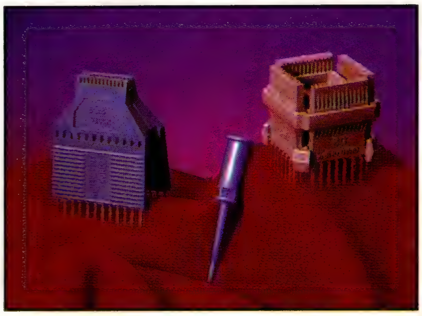

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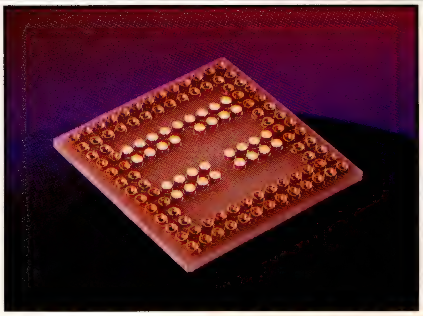

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Circle 459

UPDATE: THE DSP-CONTROLLER MARRIAGE HAS 'EM PURRING

A year after its introduction, the chip billed as "a new concept in digital signal control" has attracted hundreds of potential customers, and applications calling for a half million to a million pieces annually are in sight. No wonder, then, that both Texas Instruments Inc. and Microchip Technology Inc., joint developers of the 320C14 combination digital signal processor and microcontroller—a digital signal controller—pronounce themselves quite satisfied with the concept.

"Customers up against a problem have jumped on it rapidly," says George Rigg, vice president and general manager of Microchip's Logic Products division in Chandler, Ariz. "And a lot of others are becoming aware of how they can use it, though they need time to come up with an application and apply the chip fully." Both TI and Microchip plan full-scale production for the first quarter of next year. Eventually, parts will sell for under $10.

The 320C14 combined for the first time a DSP with the on-chip peripherals of a 16-bit microcontroller [*Electronics*, October 1988, p. 127]. Once in full production, the chip will operate at up to 25.6 MHz and execute 6.4 million instructions per second. This makes it the world's fastest microcontroller, five to 10 times speedier than traditional 16-bit microcontrollers, TI says. Almost all instructions, including multiplication, are executed in a single 160-ns cycle.

DIGITAL SIGNAL PROCESSING

TECHNOLOGY TO WATCH

AT LAST, THE MARRIAGE OF DSP WITH MICROCONTROLLER FEATURES

A single chip combines DSP speed and muscle of microcontroller peripherals

There's an important new wrinkle in the chip market: the merger of high-performance microcontrollers and digital signal processors. The product of that marriage is being called a digital signal controller, arriving in the form of the DSC320C14 developed by Microchip Technology Inc. of Chandler, Ariz., with help from its DSP second-sourcing partner, Texas Instruments Inc. of Dallas.

Targeted at real-time, closed-loop control, the 25.6-MHz integrated circuit is a 16-bit controller with tightly coupled peripheral and input/output functions normally associated with monolithic microcontrollers. It also has the number-crunching processor core of TI's 320 DSP architecture.

The DSP portion of the 320C14 executes 6 million instructions/s. The microcontroller features provide 256 by 16 bits of on-board static random-access memory and 4,096 by 16 bits of read-only memory, plus six pulse-width-modulation outputs with 50-ns resolution and four inputs for pulse detection with 160-ns resolution. Also bundled on the CMOS chip are 16 configurable I/O lines, a serial port, 16 interrupts, four 16-bit timers, and hardware support for communications protocols.

Compared with conventional microcontrollers, DSPs are somewhat like a racehorse; bred for high-speed performance. The workhorse microcontrollers, by contrast, are not usually built for speed—but they have the muscle through integrated features to tackle many jobs.

But now, high-performance control applications need both characteristics in one device: the speeds of DSP for complex mathematical calculations alongside the flexibility of microcontroller features. The latter include sophisticated I/O structures, watchdog timers, pulse-width modulated outputs, and flexible interrupt structure. Error-observant watchdog timers, for example, insure reliability when control systems must run for long periods of time. A flexible interrupt structure can be used to change software-execution sequences in response to real-time events. A flexible I/O structure is often required to deal with off-chip devices in control applications.

The 320C14 has those kinds of features and more, says Rahul Sud, marketing vice president at Microchip, which until April was the Microelectronics Division of General Instrument Corp. (see p. 133). First, he says, the digital-signal controller is four to five times faster than existing 16-bit microcontrollers. And it operates under the industry's most popular DSP instruction set—it's software-compatible with TI's prolific 32010 processor.

Moreover, its peripheral features compensate for the traditional shortcomings of DSPs in control. Along with a DSP core that has 160-ns cycle times and can exe-

Production to start at TI and Microchip in first quarter with a target price of $10

At the device's core is TI's popular TMS320C10, which handles the computations often performed by a separate DSP coprocessor. The result: a microcontroller that can be used in real-time, closed-loop digital control.

The new chip is aimed at servo control and applications requiring more performance than traditional 16-bit microcontrollers provide. Basically, a servo-control problem is a signal-processing problem, says TI applications engineer Irfan Ahmed in Houston. "What you're trying to do is process an input like a position, a velocity, a torque signal, or a current according to some kind of controller or filter algorithm," he says. "Conventional microcontrollers are not fast enough for the processing but must rely instead on look-up tables to approximate results. They just don't have the speed to execute the advanced control algorithms often needed."

The 320C14, with its DSP engine, can handle these algorithms. And with its on-chip, single-cycle, 16-by-16 multiplier and modified Harvard architecture, it can implement the algorithms in real time with the accuracy of analog-type performance.

Applications include areas such as disk and tape drives and plotters; engine control, adaptive suspension, antiskid braking, and instrumentation of automotive systems; robotics and motor control; and missile guidance and platform stabilization. Advanced control algorithms and techniques handled in real time include deadbeat, optimal, and adaptive control, state and observer models, and Kalman filtering.

An array of software and hardware tools from third-party developers has emerged during the past year. "We were really excited [about the chip] because we knew it was going to be great for the motion-control market," says Tom Bucella, president of Teknic Inc., Rochester, N. Y., a five-year-old specialist in motion-control design. Bucella first tried to get TI to pay for developing an evaluation board, "which is the way we usually work." TI declined, but Bucella decided to go ahead anyhow.

Last July, Teknic introduced its first off-the-shelf product, the Power 14 Standalone Evaluation Board for developing applications. The $1,000 board contains hardware for a complete motion-control sytem. Included is emulation hardware, a monitor/debugger program, three channels of switching servo amplifiers, and an analog-to-digital subsystem plus 320C14 chip.

Teknic also has a $995 software package with routines for implementing a dc servo indexer. Designers can pick and choose among the package's functions and rearrange them to suit their needs.

Tools from others include a $7,000 development system with in-circuit emulation from MicroWorkShop Inc., Hicksville, N. Y; and a $2,400 in-circuit emulator from Macrochip Research Inc., Dallas. Assembler/linkers, in-circuit emulators, and simulators are available from Microchip Technology and TI. Other third-party vendors include Loughborough Sound Images of Marlborough, Mass., and Emu-Sys of Minneapolis.

TI's TMS320E14 has 4,000 words of erasable programmable read-only memory in a 68-pin plastic-leaded chip carrier. A 25.6-MHz chip is due this month; somewhat slower versions have been $50 each. Coming is a one-time programmable chip in a 68-pin ceramic windowed package and the TMS320C14 with 4,000 words of ROM.

Microchip's DSC320C14 has 4 Kwords of ROM in a 40-lead plastic dual in-line package and in 44- and 68-lead PLCCs. Its 15-, 18-, and 20-MHz versions are $15 to $20, depending on speed and volume. A 25.6-MHz version will be sampled in January. *–Alfred Rosenblatt*

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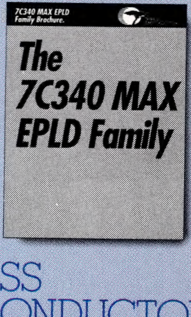

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